Using & Getting Benefit From SMF 113 Records Customer Experience

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Garanti Technology

3/3/2011
8531

Agenda

- Who is GT
- GT Mainframe Configuration
- z10 & z196 CPU Cache Architecture
- SMF 113 Counters' Meanings
- LSPR Terms
- z10 To z196 Upgrade Performance Analiz Using SMF113 Counters
- Explaining Daily & Periodic Performance Behaviours Using SMF113 Counters

WHO IS GT ?

Who is GT ?

GARANTI TECHNOLOGY

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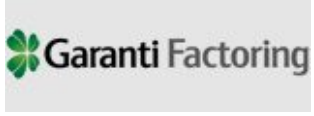
- A wholly-owned subsidiary of Garanti Bank, the second largest private bank in Turkey owned by Doğuş Group and BBVA.
- One of the largest private internal IT service providers in Turkey
- Most up-to-date IT infrastructure
- Tightly integrated and fully in-house developed, custom-fit IT solutions
- Uninterrupted transaction capability and infrastructure security
- Well-reputed as a company of “firsts”
- Visionary and continuous investment in technology since 90’s

Business & IT Alignment

Garanti

- Fast decision making and strong communication from top to down
- Centralized management reporting systems, enable management to take timely actions
- Advanced CRM applications
- Paperless banking

Who is GT ?



DOĞUŞ GRUBU

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Who is GT ?

Branch Network

- 795 Branches
- Presence in 72 Cities:
- 89% Geographic Coverage

Internet Banking

- ~1.3 MM Internet Bank Active Customers
- Recognized As Turkey's Best Internet Bank

Credit Cards

- >7,9 mn credit cards
- >355,000 POS devices
- Loyalty program for 9 banks

ATM

- 2,766 ATMs
- Cardless Transactions
- Coin Dispenser

Mobilebank

- 1st in the World to Allow Money Transfer Via SMS
- wap.garanti.com.tr --1st internet bank access via mobile in TR w/o application downloads or activations

Contact Center

- >3.4 mn Calls/mo
- 2009 Sales >2,7 mn Products
- CTI & Workforce Man.
- World's 1st to receive
- "EFQM Award"

ccf EUROPEAN CALL CENTRE AWARDS 2008 winner

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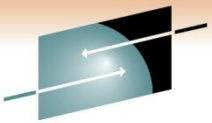
GT Is A Member Of …

- SHARE

- CMG

- GDPS Design Council
- zBLC

GT – Mainframe Configuration



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GAR2
IBM System z196 2817-717

1816 MSU
17 GCP 1 zIIP
2 ICF
165 GB Memory
32 Ficon Exp8
Crypto Express3
6 Infiniband
5p OSAE3 GbE SR
3 p OSAE3 1000Base T
4 p OSAE3 GbE SX
4 ISC-3 link

2 McData 6140

GAR1
IBM System z196 2817-717

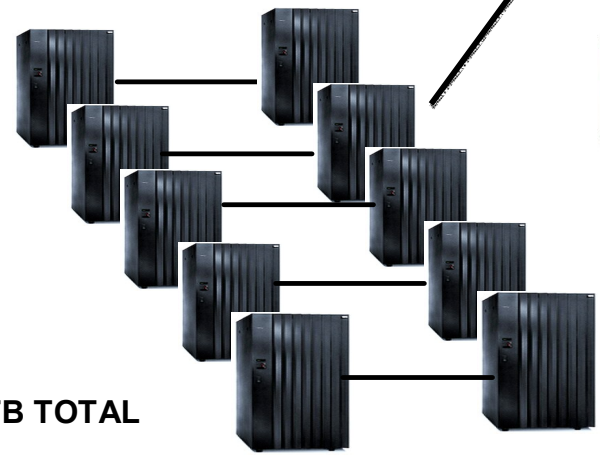
1816 MSU
17 GCP 2 zIIP
2 ICF
165 GB Memory
32 Ficon Exp8
Crypto Express3
6 Infiniband
5p OSAE3 GbE SR
3 p OSAE3 1000Base T
4 p OSAE3 GbE SX
4 ISC-3 link

z/OS 1.10
CICS TS 3.2
DB2 V9

IRD

HiperDispatch

GCL



134 TB TOTAL

6 INFO4100 Printer

IBM TS7740 Virtual Tapes

TS7740 Grid

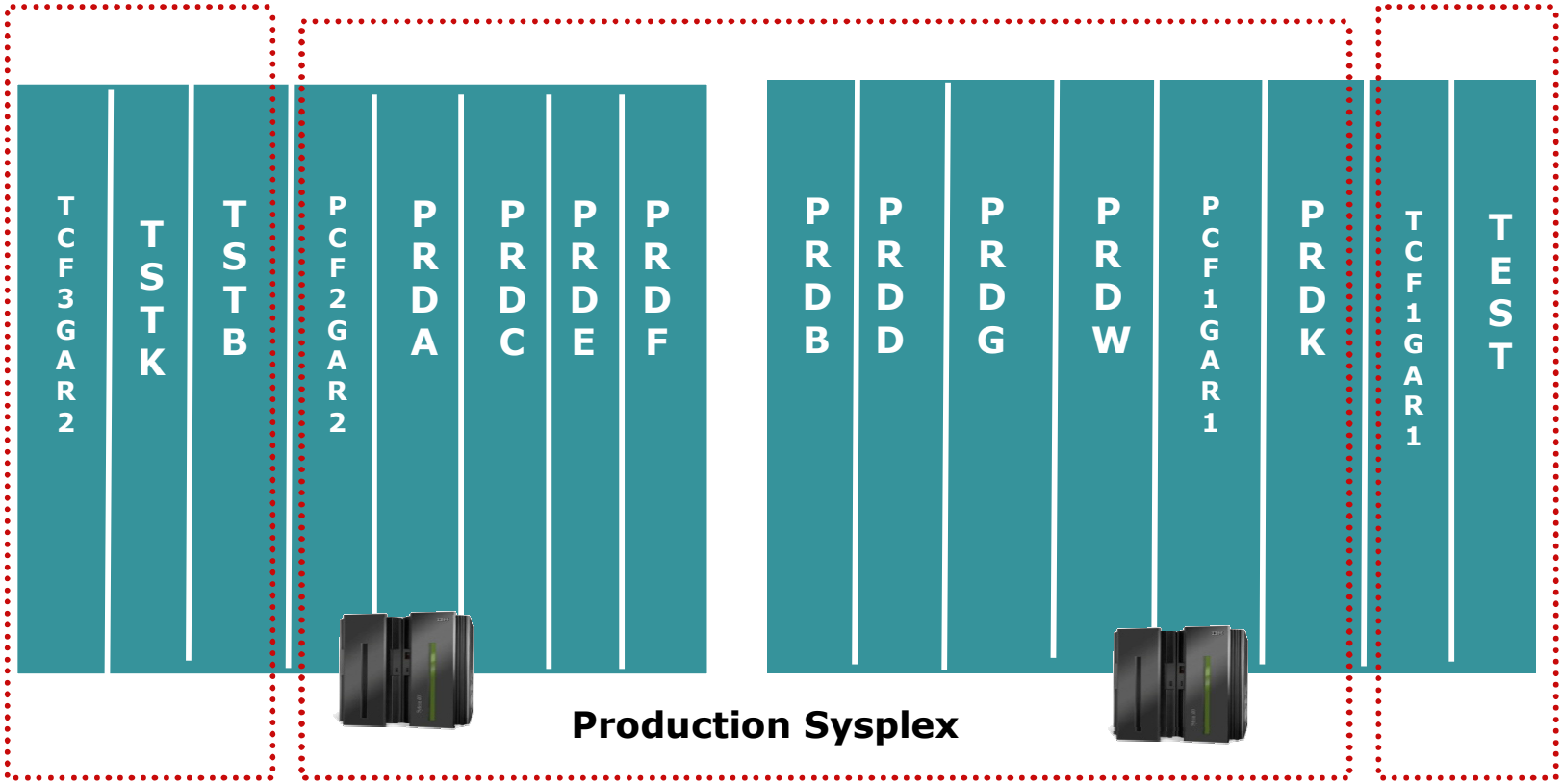
IBM TS3500 Tape Libraries

DS8700 & DS8300 Turbo
PPRC & XRC Primary

GDPS PPRC
Hyperswap Manager

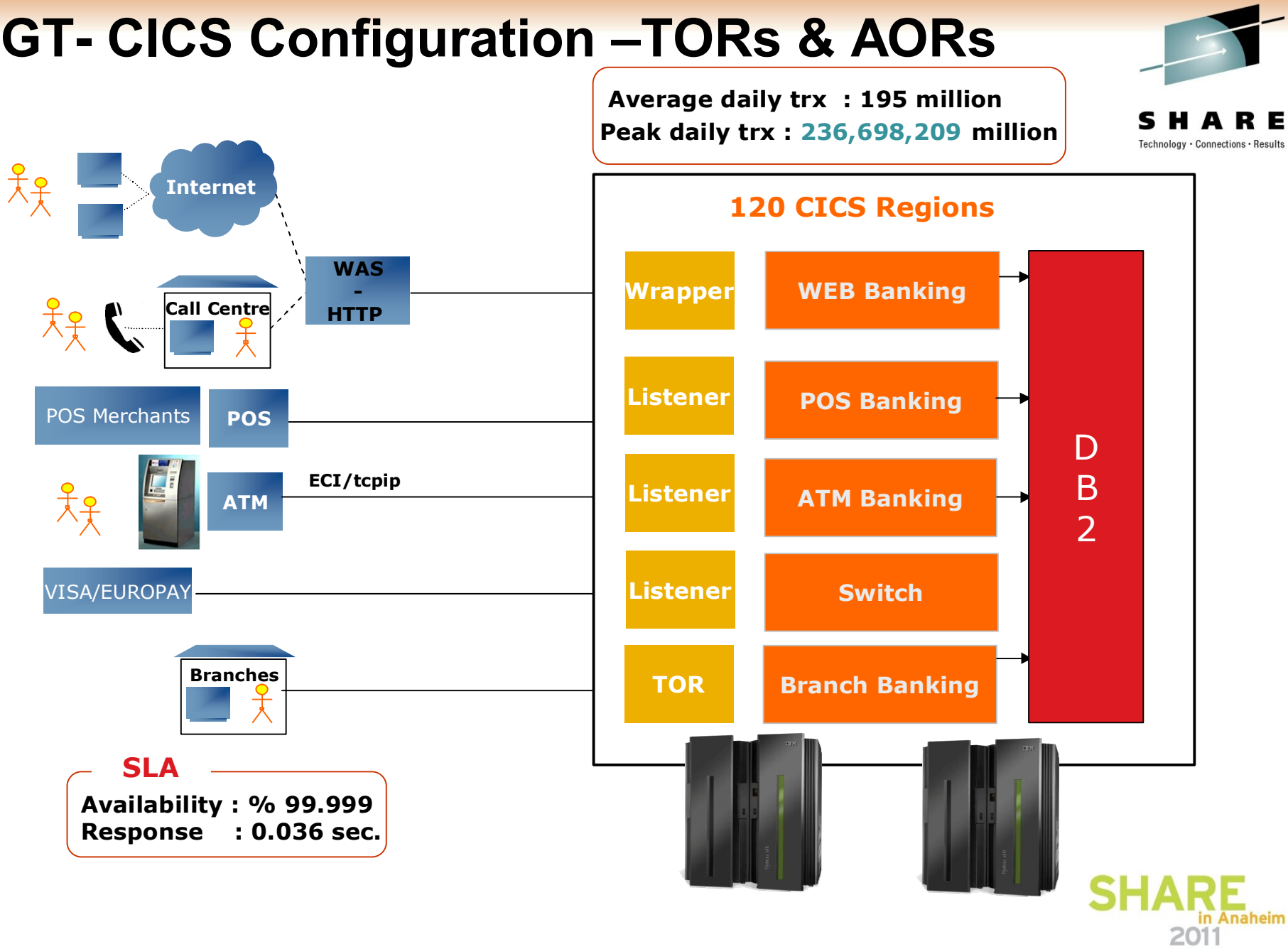
DS8700 & DS8300 Turbo
PPRC & XRC Primary

GT- z/OS Configuration



z/OS 1.10
DB2 V9
CICS TS 3.2

GT- CICS Configuration –TORs & AORs



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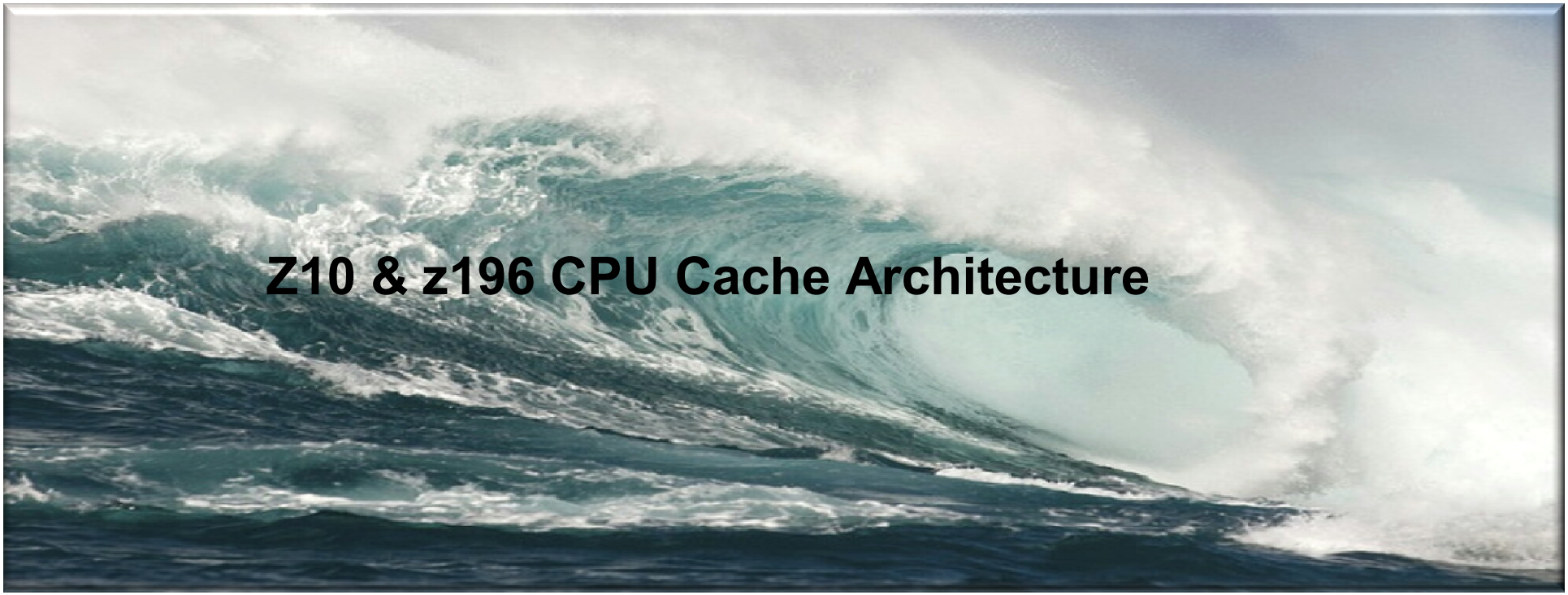
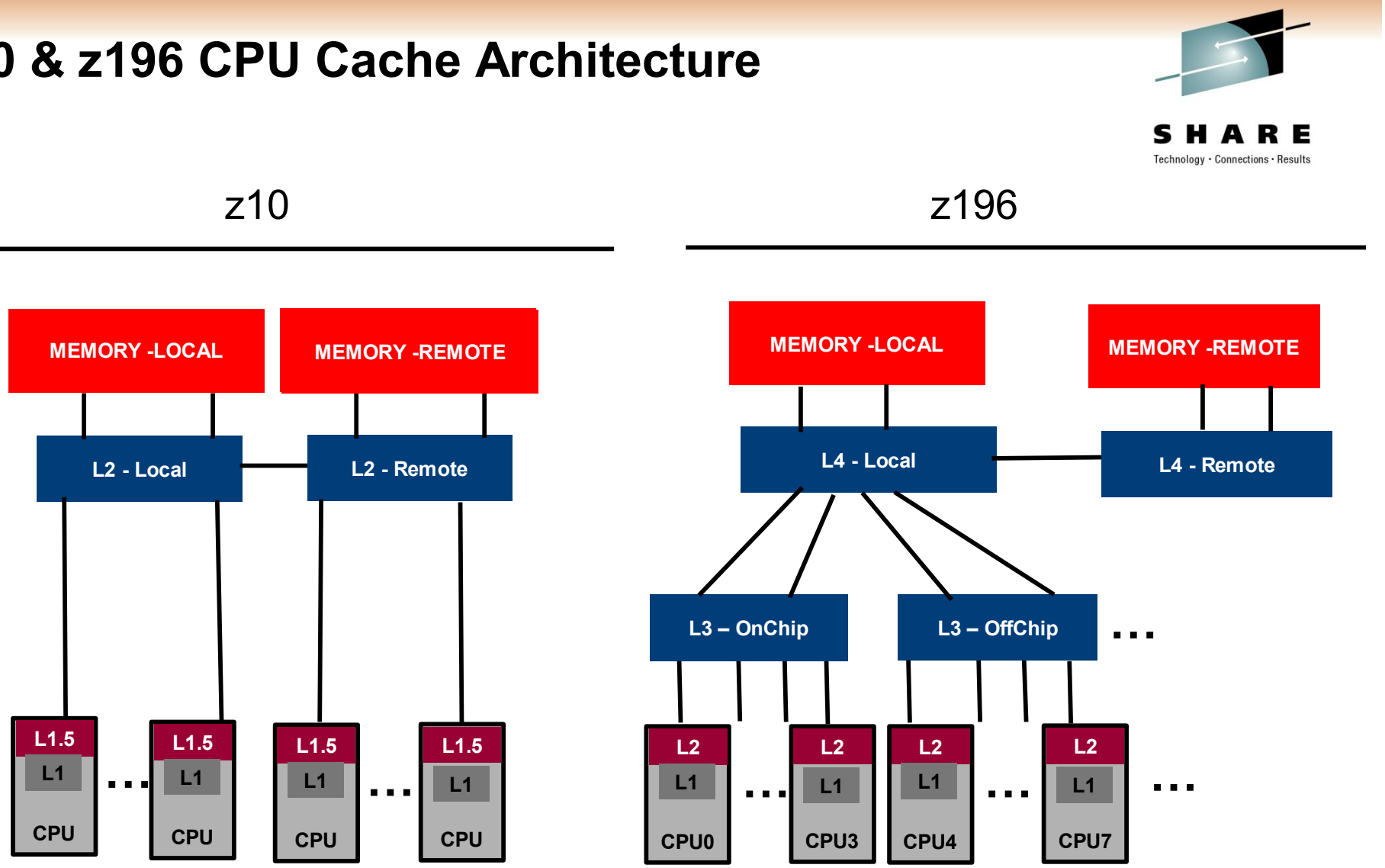
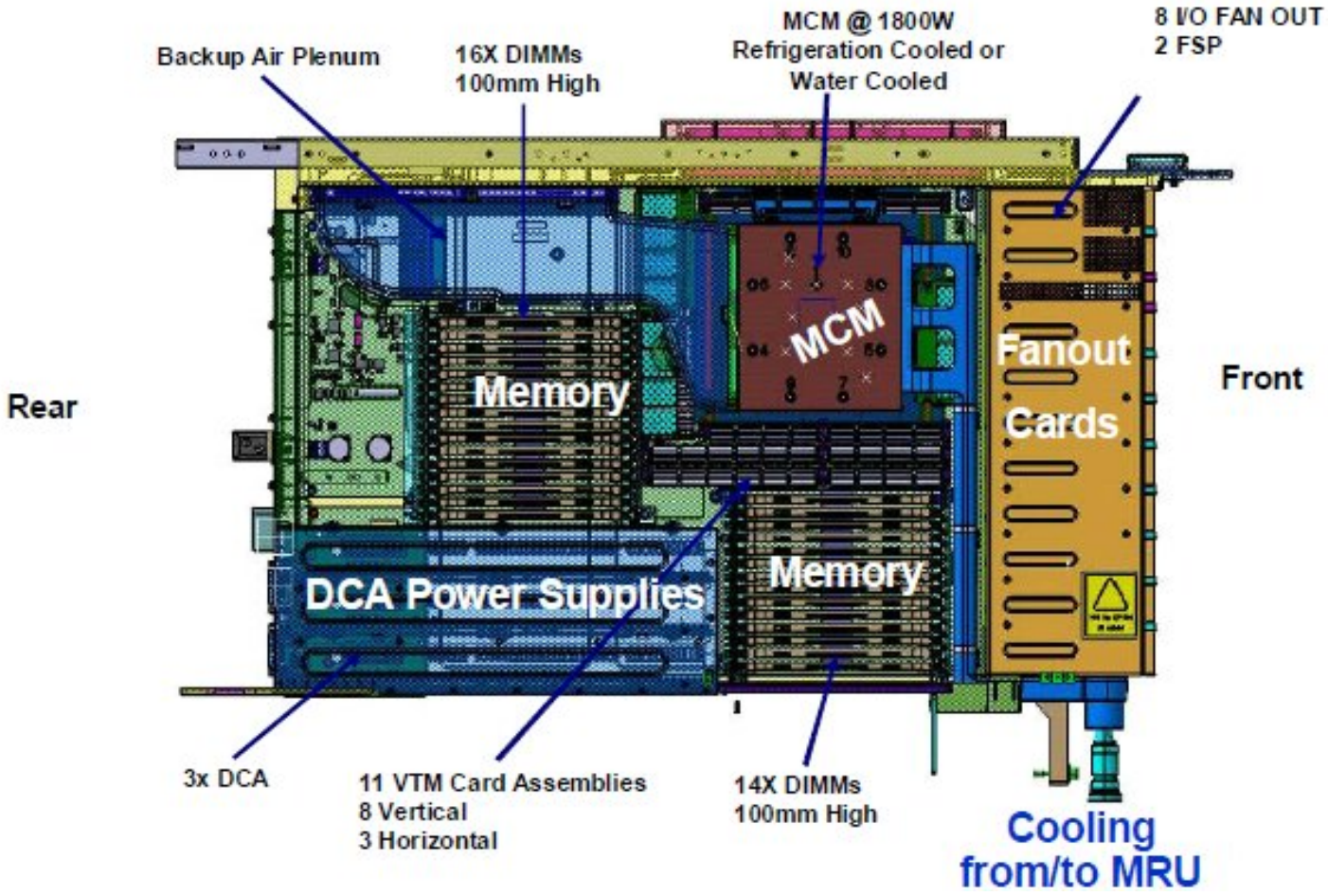
Z10 & z196 CPU Cache Architecture



Z10 & z196 CPU Cache Architecture

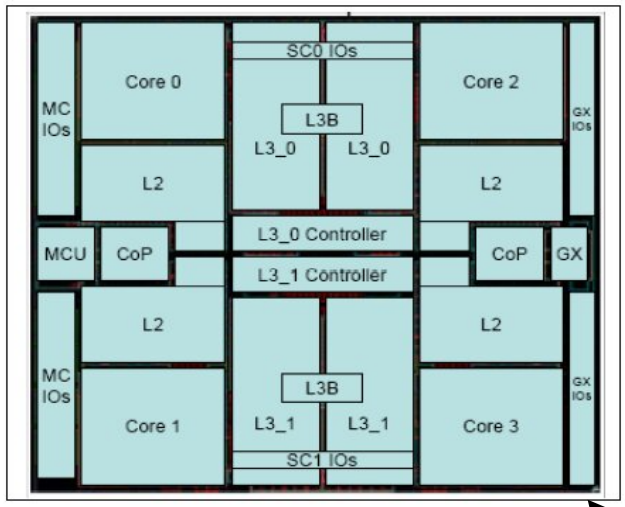


z196 Book


Backup Air Plenum
16X DIMMs
100mm High
MCM @ 1800W
Refrigeration Cooled or
Water Cooled
8 I/O FAN OUT
2 FSP
Rear
Front
Memory
MCM
Fanout
Cards
DCA Power Supplies
Memory
3x DCA
11 VTM Card Assemblies
8 Vertical
3 Horizontal
14X DIMMs
100mm High
Cooling
from/to MRU

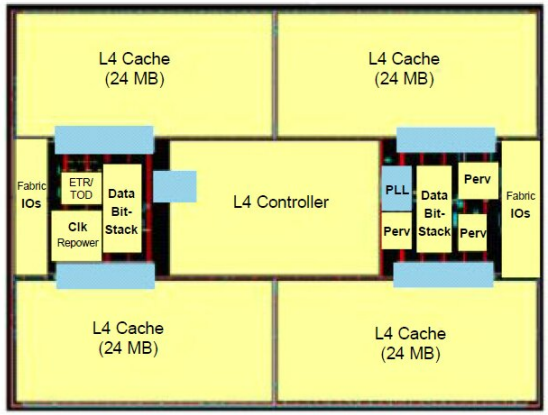
z196 Book – Top To Down Approach

Z196 Quad Core PU Chip



In each PU chip
4 PCPs

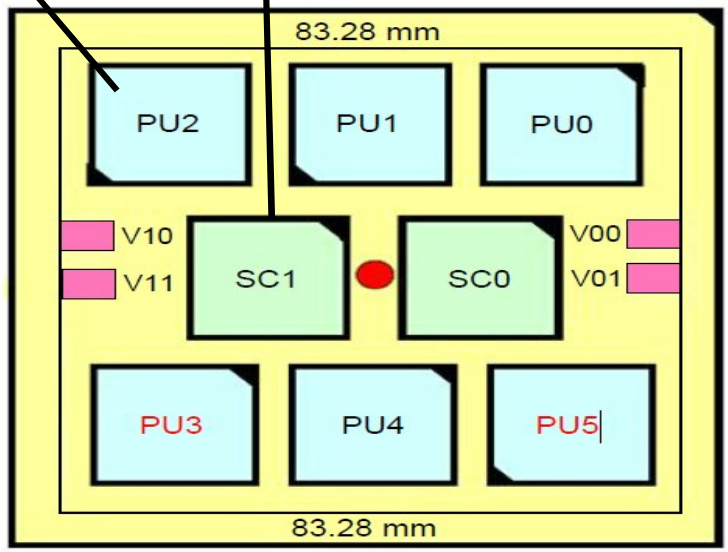
Z196 SC(Storage Controller) Chip – 96 MB



In each MCM 2 SC Chips

Book

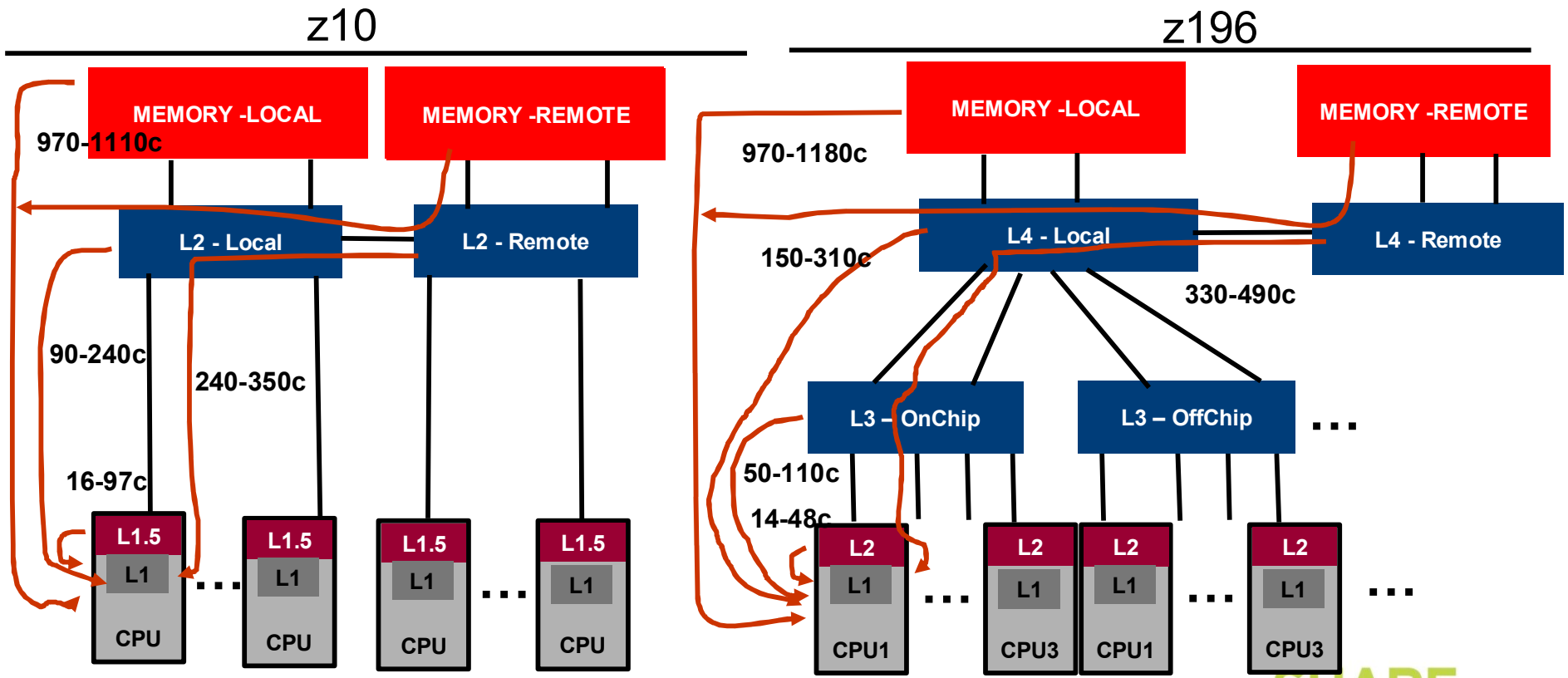
Z196 MCM



One Book
6 PU Chips

z10 & z196 Cache Distance - CPU Cycles & CPU Time

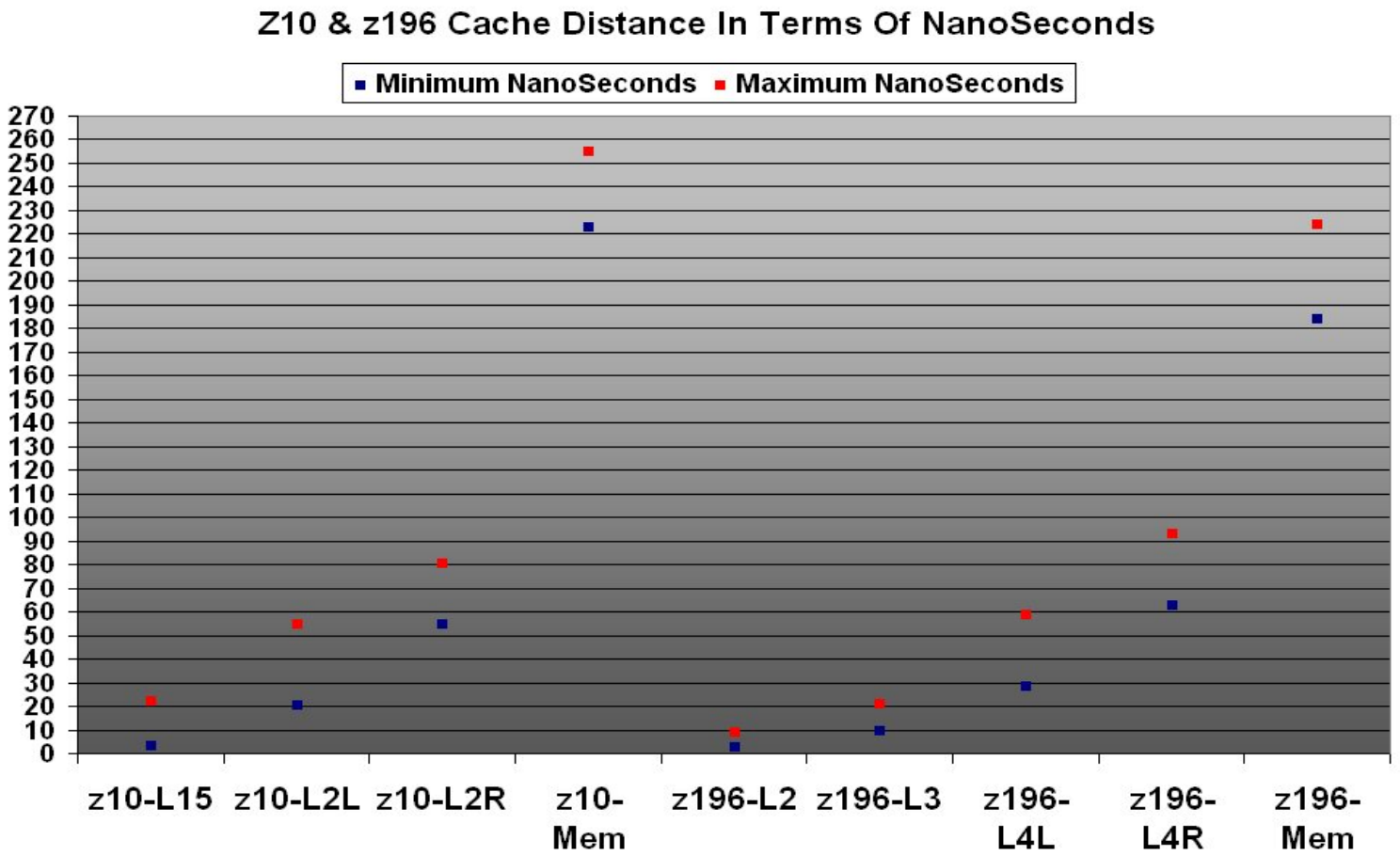
Z10 Caches & Memory Latency	zG Caches & Memory Latency
L1 (CPU, 64K I/128K D)	L1 (CPU 64K I/ 64K-128K D)
L1.5 (CPU, 3M, 16-97c)	L2 (CPU, 1.5M, 14-48c)
----------N / A----------	L3 (Chip, 24M, 50-110c)
Local L2 (Book, 48M, 90-240c)	Local L4 (Book, 192M, 150-310c)
Remote L2 (Book, 240-350c)	Remote L4 (Book, 330-490c)
Memory (970-1110c)	Memory (970-1180c)



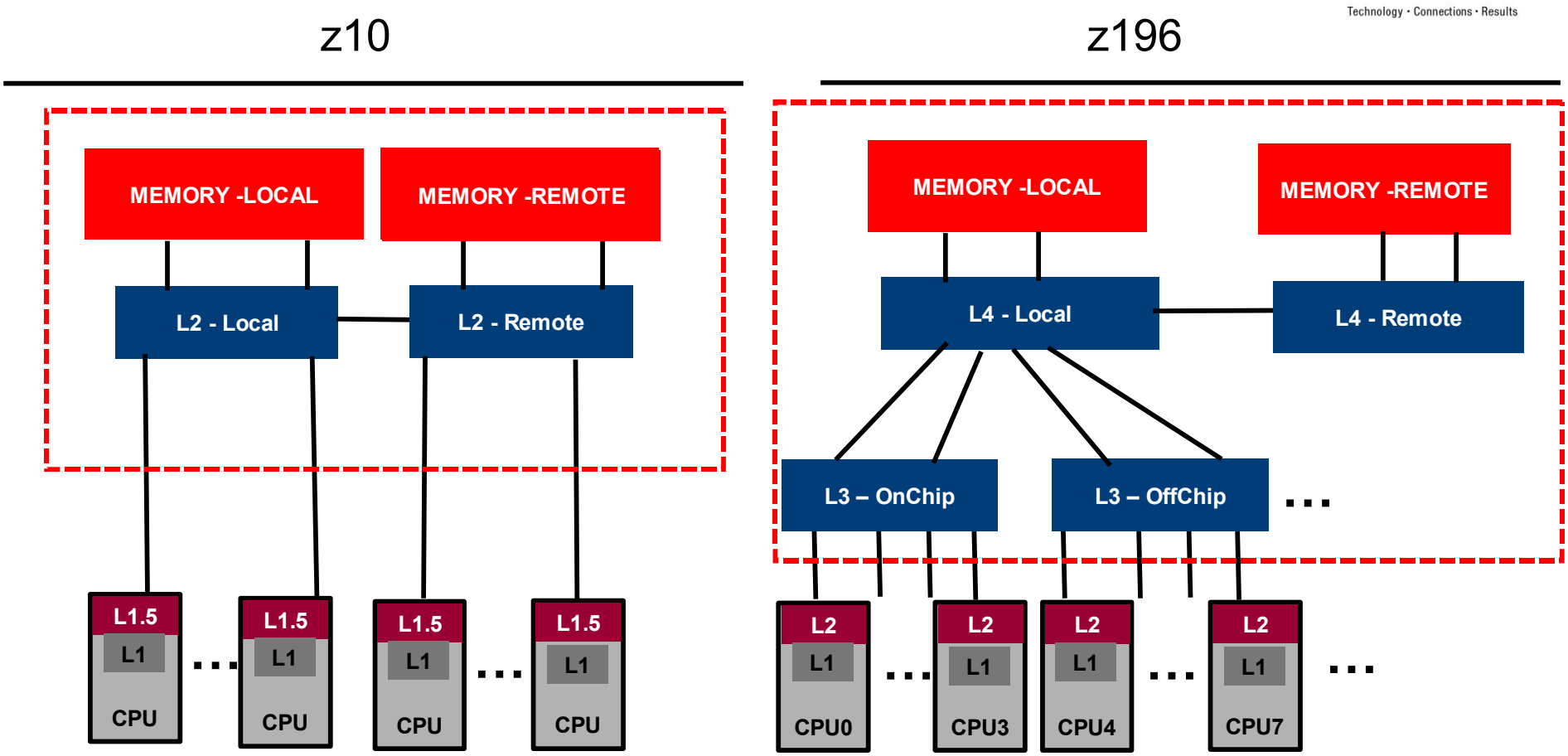
z10 & z196 Cache Distance - CPU Cycles & CPU Time

Z10 4.4 GHz 0.23 ns → 18 % → Z196 5.2 GHz 0.19 ns

Increase In Cycle Speed

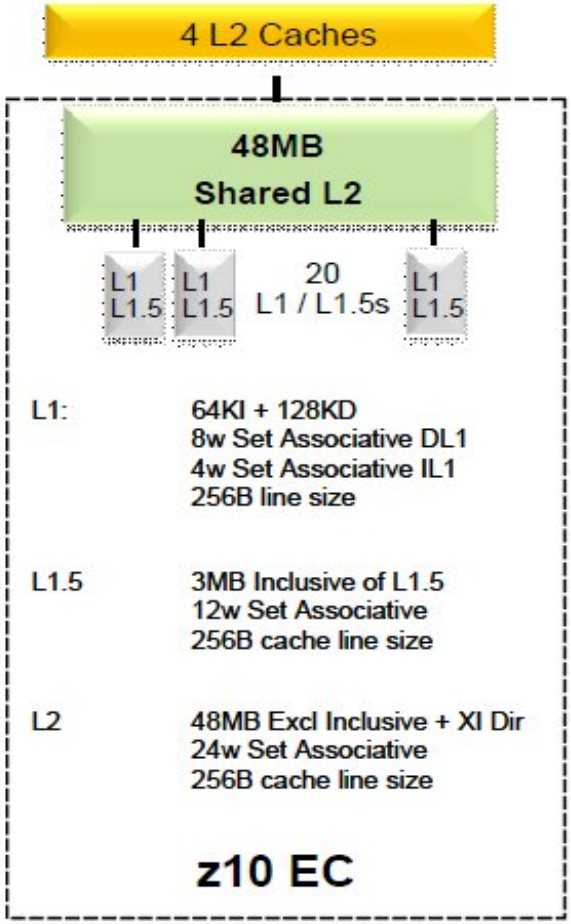


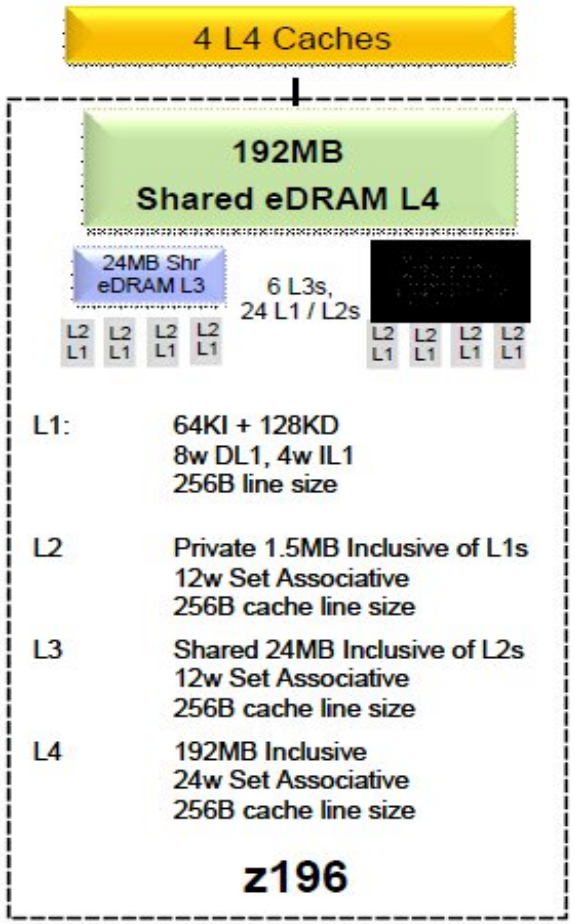
z10 & z196 NEST



z10 & z196 Cache Sizes

- **z196 L2 is %50 Smaller Than z10 L1.5 Cache**
- **Cache Line Size Is SAME = 256B In Both Models.**






SMF 113 COUNTERS

SMF 113 Counters – BASIC COUNTERS (z10 & z196)

BASIC00 : Cycle Count
BASIC01 : Instruction Count

BASIC02 : L1-Instruction Cache Directory Write Count
BASIC04: L1- Data Cache Directory Write Count

BASIC03 : L1-Instruction Cache Penalty Cycle Count
BASIC05: L1-Data Cache Penalty Cycle Count

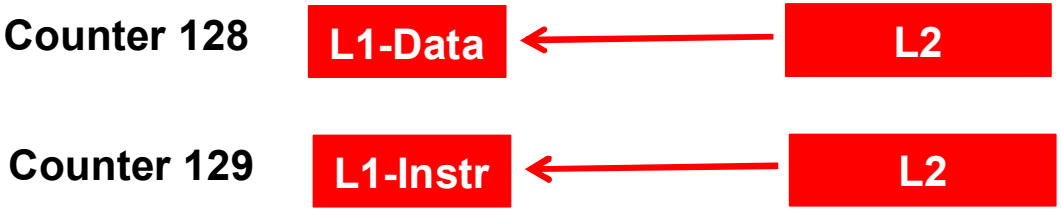
PROBST32 : Problem State Cycle Count
PROBST33 : Problem State Instruction Count

PROBST34 : Problem State L1-I Cache Directory Write Count
PROBST35 : Problem State L1-I Cache Penalty Count

PROBST36 : Problem State L1-D Cache Directory Write Count
PROBST37 : Problem State L1-D Cache Penalty Count

…

SMF 113 Counters – EXTENDED COUNTERS (z196)



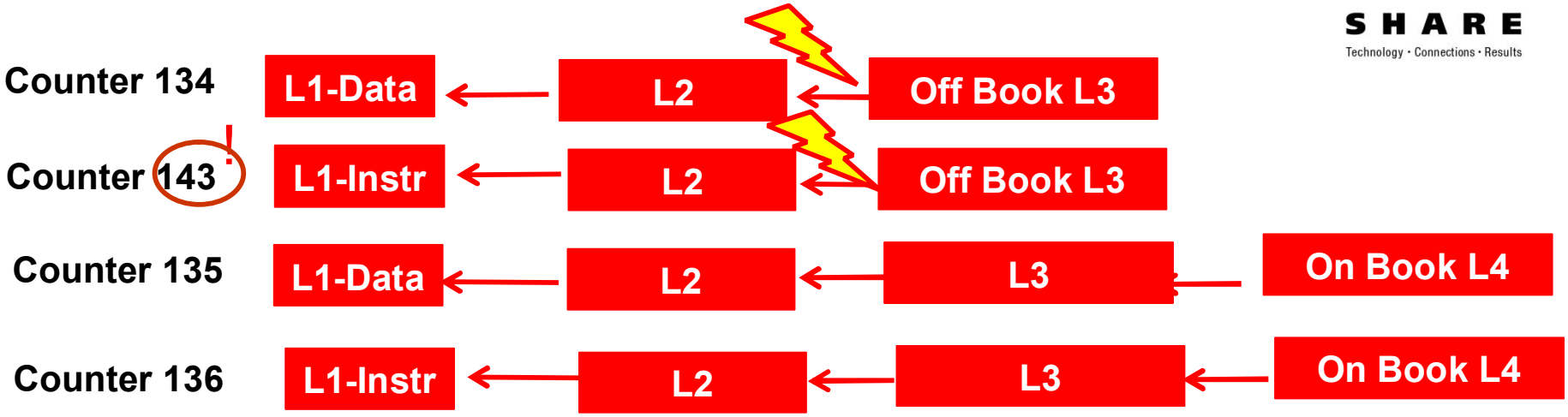
Counter 130 – Level-1 Data TLB miss in progress.
Incremented by one for every cycle a DTLB1 miss is in progress.

Counter 131 – Level-1 Instr TLB miss in progress.
Incremented by one for every cycle an ITLB1 miss is in progress.

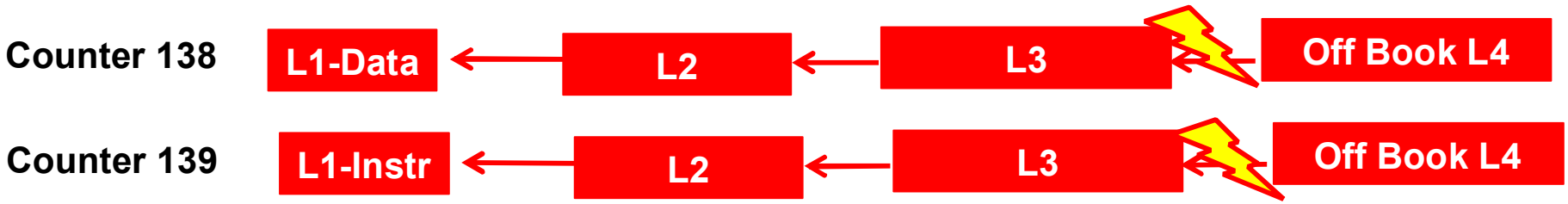
Counter 132 – Undefined

Counter 133 - Incremented by one for every store sent to Level-2 cache

SMF 113 Counters – EXTENDED COUNTERS (z196)

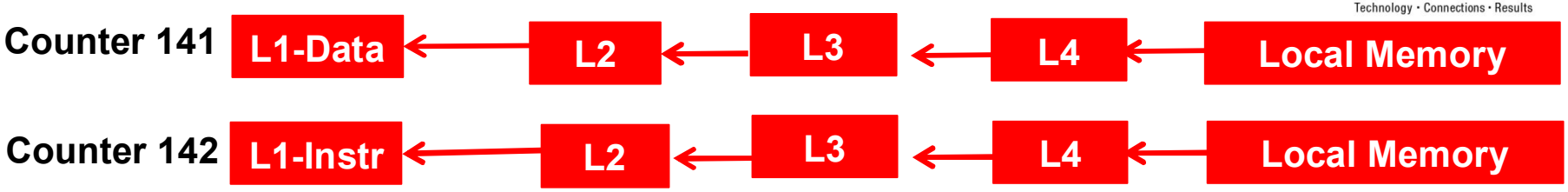


Counter 137 – A directory write to the Level-1 Data cache where the line was originally in a Read-Only state in the cache but has been updated to be in the Exclusive state that allows stores to the cache line.



Counter 140 - A translation entry has been written to the Level-1 Data Translation Lookaside Buffer for a one-megabyte page.

SMF 113 Counters – EXTENDED COUNTERS (z196)



Counter 144 – A translation entry has been written to the Level-1 Data Translation Lookaside Buffer (DTLB1).

Counter 145 – A translation entry has been written to the Level-1 Instruction Translation Lookaside Buffer (ITLB1).

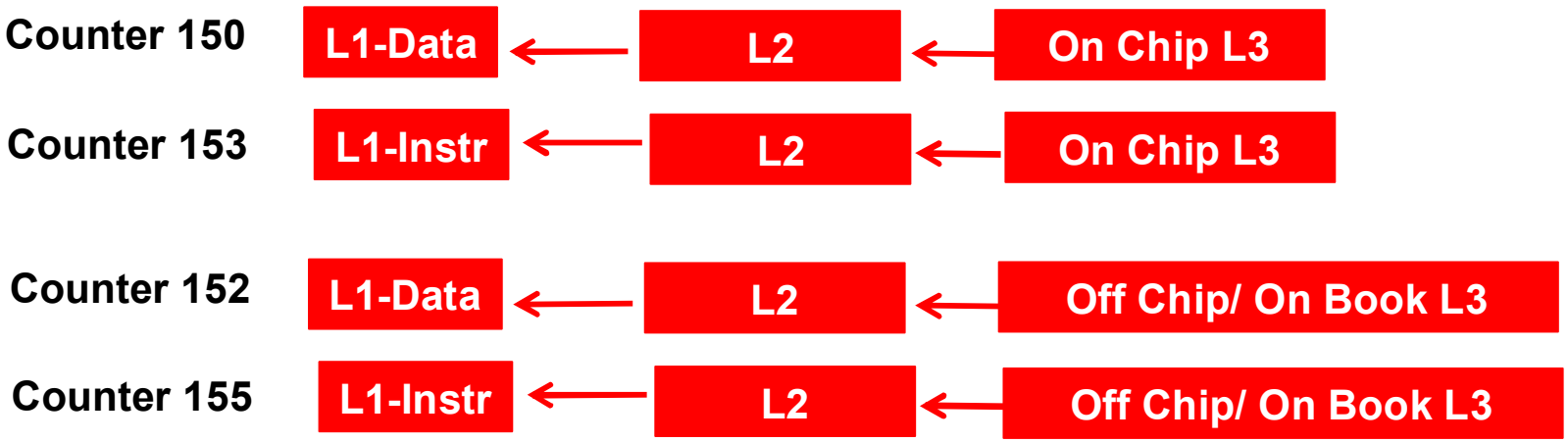
Counter 146 – A translation entry has been written to the Level-2 TLB Page Table Entry arrays.

Counter 147 – A translation entry has been written to the Level-2 TLB Common Region Segment Table Entry arrays for a one-megabyte large page translation.

Counter 148 – A translation entry has been written to the Level-2 TLB Common Region Segment Table Entry arrays.

Counter 149 – Undefined.

SMF 113 Counters – EXTENDED COUNTERS (z196)

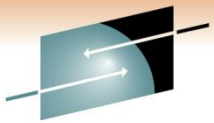


Counter 151 – Undefined

Counter 154 – Undefined

Counter 156 – Undefined

SMF 113 Counters – BASIC & Extended



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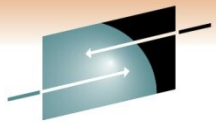
EXTENDED COUNTERS – Full (z196)

Counter 128 - A directory write to the Level-1 Data cache directory where the returned cache line was sourced from the Level-2 cache.
Counter 129 - A directory write to the Level-1 Instruction cache directory where the returned cache line was sourced from the Level-2 cache.
Counter 130 - Level-1 Data TLB miss in progress. Incremented by one for every cycle a DTLB1 miss is in progress.
Counter 131 - Level-1 Instruction TLB miss in progress. Incremented by one for every cycle an ITLB1 miss is in progress.
Counter 132 - Undefined.
Counter 133 - Incremented by one for every store sent to Level-2 cache.
Counter 134 - A directory write to the Level-1 Data cache directory where the returned cache line was sourced from an Off Book Level-3 cache.
Counter 135 - A directory write to the Level-1 Data cache directory where the returned cache line was sourced from an On Book Level-4 cache.
Counter 136 - A directory write to the Level-1 Instruction cache directory where the returned cache line was sourced from an On Book Level-4 cache.
Counter 137 - A directory write to the Level-1 Data cache where the line was originally in a Read-Only state in the cache but has been updated to be in the Exclusive state that allows stores to the cache line.
Counter 138 - A directory write to the Level-1 Data cache directory where the returned cache line was sourced from an Off Book Level-4 cache.
Counter 139 - A directory write to the Level-1 Instruction cache directory where the returned cache line was sourced from an Off Book Level-4 cache.
Counter 140 - A translation entry has been written to the Level-1 Data Translation Lookaside Buffer for a one-megabyte page.
Counter 141 - A directory write to the Level-1 Data cache where the installed cache line was sourced from memory that is attached to the same book as the Data cache (Local Memory).
Counter 142 - A directory write to the Level-1 Instruction cache where the installed cache line was sourced from memory that is attached to the same book as the Instruction cache (Local Memory).
Counter 143 - A directory write to the Level-1 Instruction cache directory where the returned cache line was sourced from an Off Book Level-3 cache.
Counter 144 - A translation entry has been written to the Level-1 Data Translation Lookaside Buffer (DTLB1).
Counter 145 - A translation entry has been written to the Level-1 Instruction Translation Lookaside Buffer (ITLB1).
Counter 146 - A translation entry has been written to the Level-2 TLB Page Table Entry arrays.
Counter 147 - A translation entry has been written to the Level-2 TLB Common Region Segment Table Entry arrays for a one-megabyte large page translation.
Counter 148 - A translation entry has been written to the Level-2 TLB Common Region Segment Table Entry arrays.
Counter 149 - Undefined.
Counter 150 - A directory write to the Level-1 Data cache directory where the returned cache line was sourced from an On Chip Level-3 cache.
Counter 151 - Undefined.
Counter 152 - A directory write to the Level-1 Data cache directory where the returned cache line was sourced from an Off Chip/On Book Level-3 cache.
Counter 153 - A directory write to the Level-1 Instruction cache directory where the returned cache line was sourced from an On Chip Level-3 cache.
Counter 154 - Undefined.
Counter 155 - A directory write to the Level-1 Instruction cache directory where the returned cache line was sourced from an Off Chip/On Book Level-3 cache.
Counter 156 - Undefined.
To derive approximate rates for remote memory on Systems with more than one Book:
Directory writes to the Level-1 Instruction cache that was sourced from Remote Memory = Counter 2 - (Counter 129+136+139+142+143+153+155)
Directory writes to the Level-1 Data cache that was sourced from Remote Memory = Counter 4 - (Counter 128+134+135+138+141+150+152)

What do SMF113 Formulas Actually Mean ?



It is Possible To Create Formulas Based On SMF113 Basic & Extended Counters Considering Meaning Of Each Counter. IBM Shared The Following:

Cycle Per Instruction (CPI)

Relative Nest Intensity (RNI)

Problem State %

L1 Miss %

% Of Data+Instr Sourced From L2
% Of Data+Instr Sourced From L3
% Of Data+Instr Sourced From L4 Local
% Of Data+Instr Sourced From L4 Remote
% Of Data+Instr Sourced From Memory Local
% Of Data+Instr Sourced From Memory Remote

You can use calculation in IBM CMF Documents To Calculate Local & Remote Memory Seperately

TOTAL MUST BE 100

What do SMF113 Formulas Actually Mean ?

LPARCPU

Estimated Instruction Complexity CPI

Estimated Finite CPI

Estimated Sourcing Cycles Per L1 Miss

Effective GHz

TLB1 CPU Miss % Of TLB Miss

TLB1 Cycles Per TLB Miss

PTE % Of All TLB1 Misses

AND

Penalty Cycles Percentage

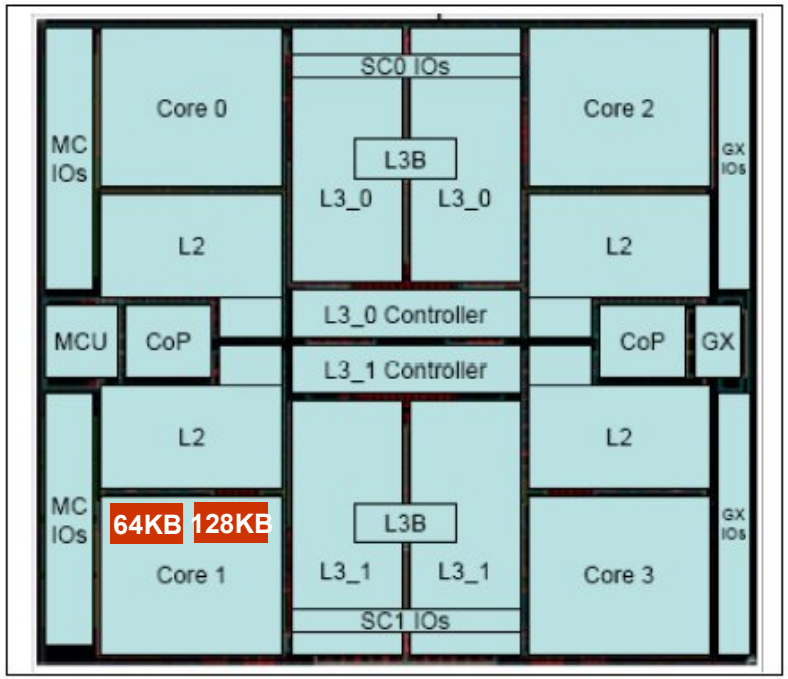
What do SMF113 Formulas Actually Mean ?

Cycle Per Instruction

$$CPI = \frac{\text{Cycle Count (B0)}}{\text{Instruction Count (B1)}}$$

Z196 Formulas – L1 Cache Miss % (L1MP)

$$L1MP = \frac{\text{L1-I Cache Directory Write Count(B2) + L1-D Cache Directory Write Count(B4)}}{\text{Instruction Count (B1)}}$$



Z196 Formulas – Sourced From L2 Cache % (L2P)

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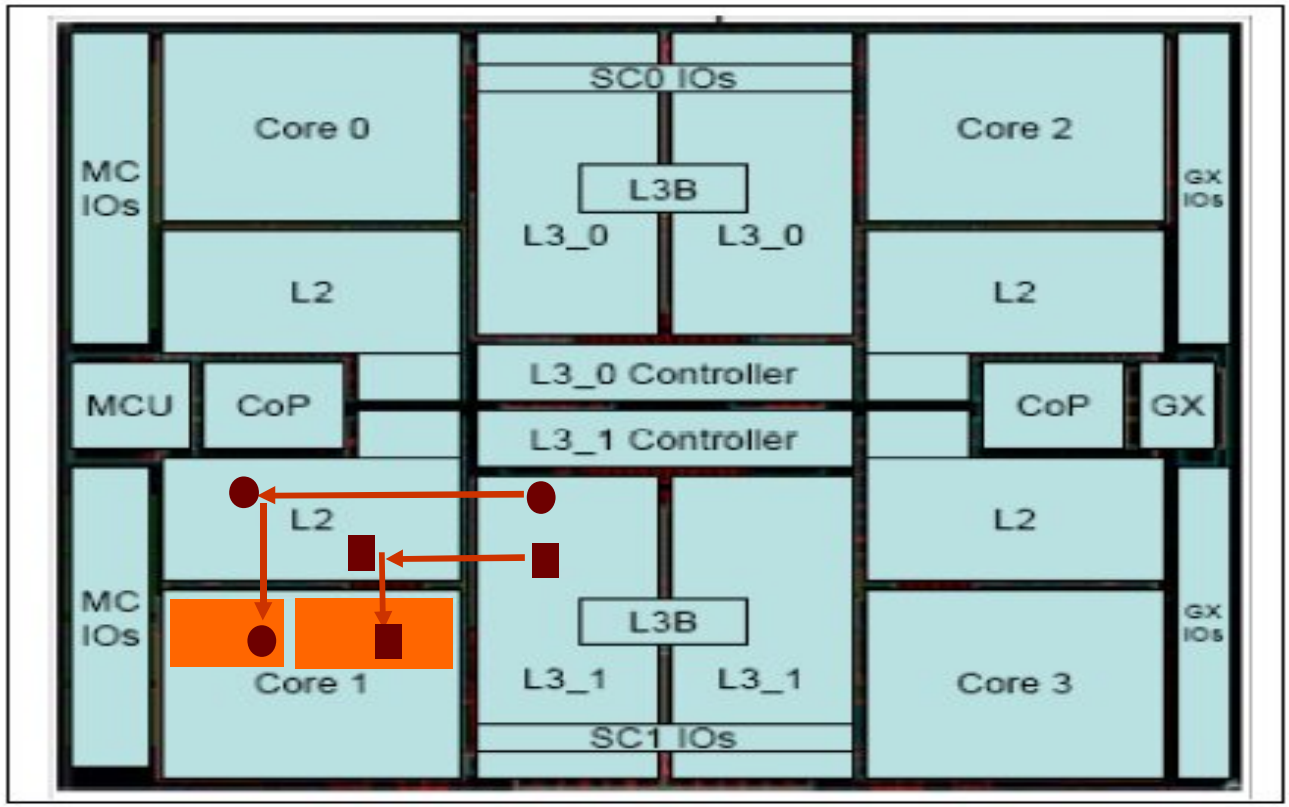
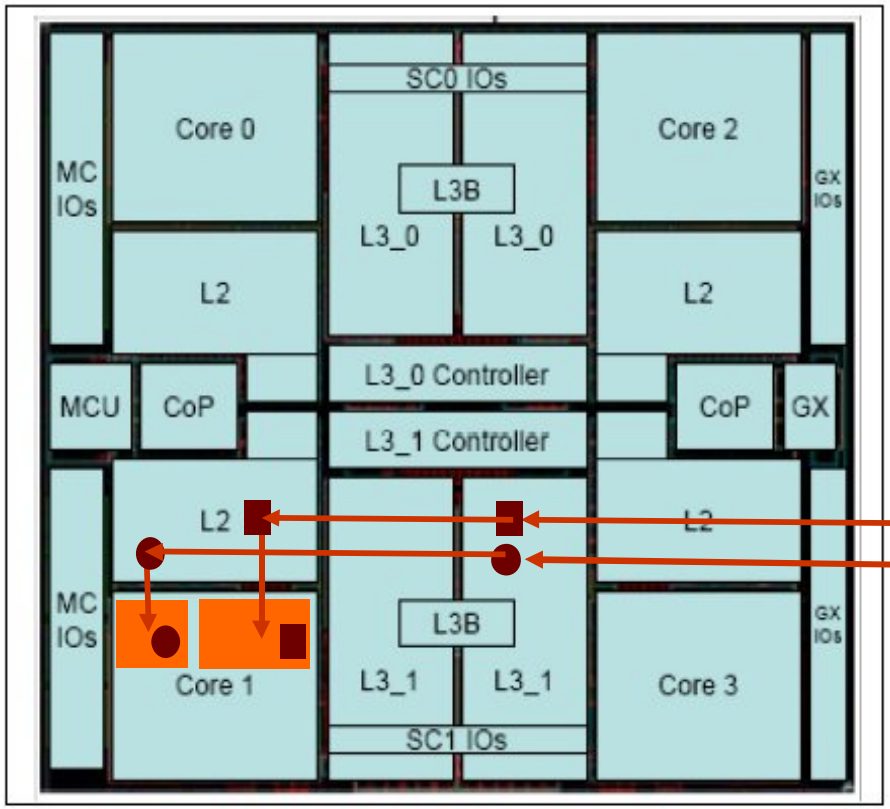
$$L2P = \frac{\text{Count of Writes To L1-D Cache Directory Sourced From L2(E128) + Count of Writes To L1-I Cache Directory Sourced From L2(E129) +}}{\text{Count of Writes To L1-I Cache Directory (B2) +Count of Writes To L1-D Cache Directory (B4)}}$$

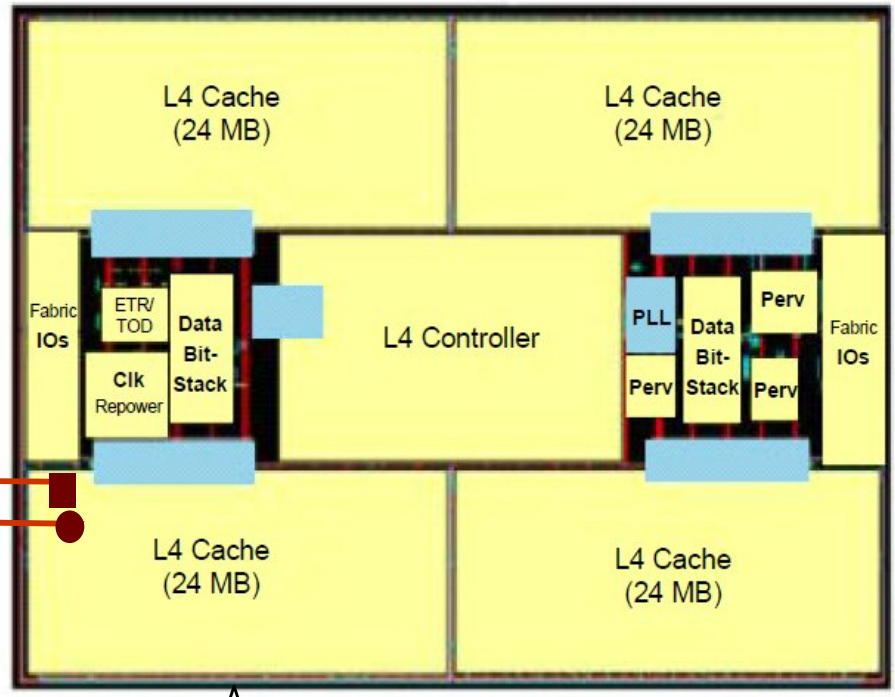
Z196 Formulas – Sourced from L3 Cache % (L3P)

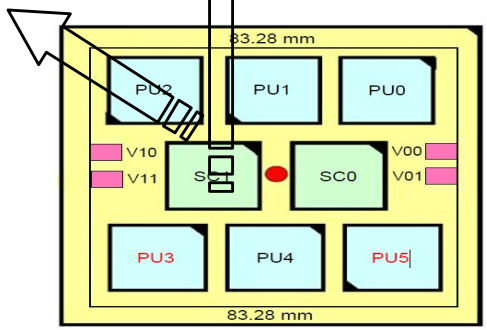
$$L3P = \frac{\text{Count of Writes To L1-I Cache Directory Sourced From On Chip L3(E150)} + \text{Count of Writes To L1-D Cache Directory Sourced From On Chip L3(E153)} +}{\text{Count of Writes To L1-I Cache Directory (B2)} + \text{Count of Writes To L1-D Cache Directory (B4)}}$$



Z196 Formulas- Sourced From L4 Local Cache% (L4LP)







Z196 Formulas- Sourced From Local L4 Cache% (L4LP)

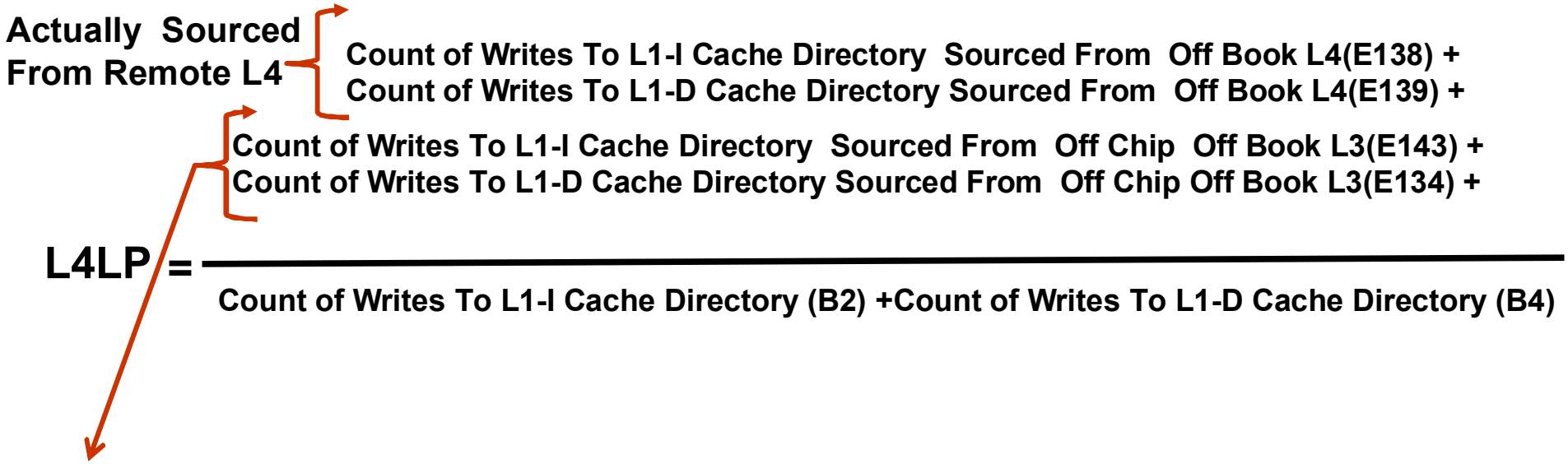
Actually Sourced From Local L4

Count of Writes To L1-I Cache Directory Sourced From On Book L4(E135) +
Count of Writes To L1-D Cache Directory Sourced From On Book L4(E136) +
Count of Writes To L1-I Cache Directory Sourced From Off Chip On Book L3(E152) +
Count of Writes To L1-D Cache Directory Sourced From Off Chip On Book L3(E155) +

$$L4LP = \frac{\text{Actually Sourced From Local L4}}{\text{Count of Writes To L1-I Cache Directory (B2) + Count of Writes To L1-D Cache Directory (B4)}}$$

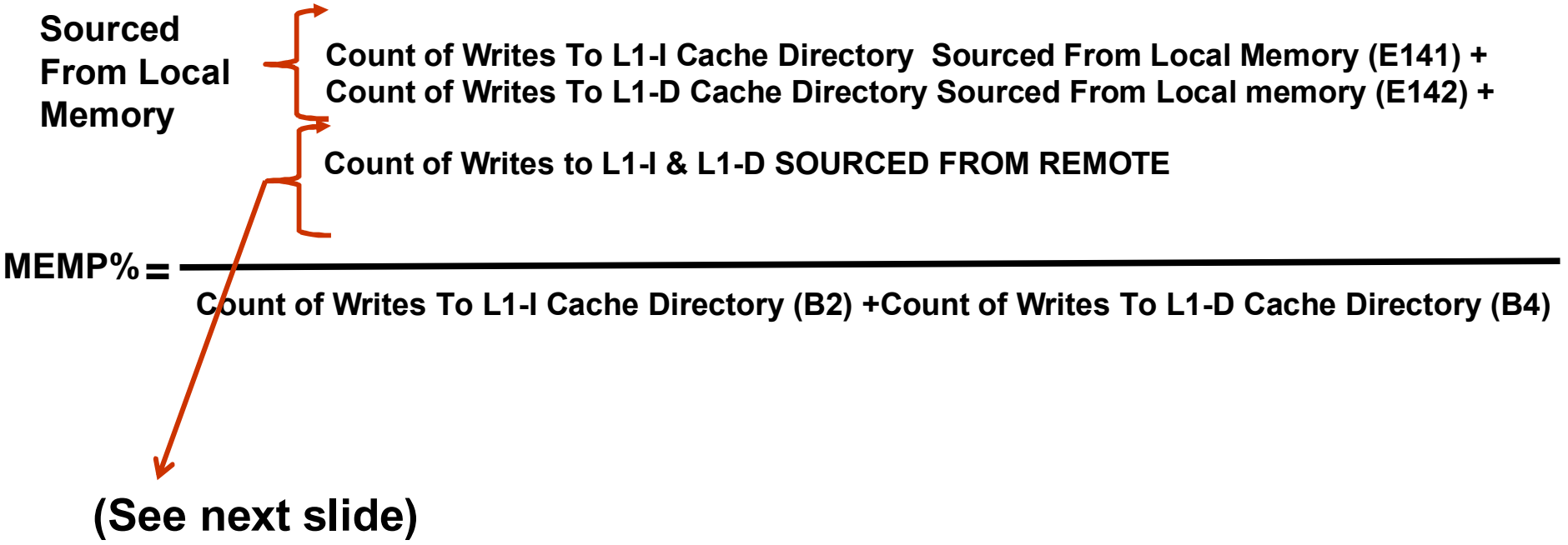
OffChip OnBook L3 is also included because there is no connection between L3 To L3
Data Should be Read From Local L4

Z196 Formulas- Sourced From Remote L4 Cache % (L4LP)

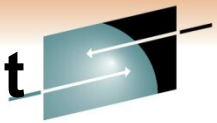


OffChip OffBook L3 is also included because same data should exist in Remote L4 Data Should be Read From Remote L4

Z196 Formulas Sourced From Memory % (MEMP)



Z196 Formulas Sourced From Remote Memory Count



Therefore SOURCED FROM REMOTE MEMORY Count =

(Count of Writes To L1-I Cache Directory (B2) +
Count of Writes To L1-D Cache Directory (B4)) –

→ **ALL Writes To L1 D&I Cache**

–

(Count of Writes To L1-I Cache Directory Sourced From L2(E128) +
Count of Writes To L1-I Cache Directory Sourced From L2(E129) +

Sourced From L2

–

Count of Writes To L1-I Cache Directory Sourced From On Chip L3(E150) +
Count of Writes To L1-D Cache Directory Sourced From On Chip L3(E153))

Sourced From L3

–

Count of Writes To L1-I Cache Directory Sourced From Off Chip Off Book L3(E143) +
Count of Writes To L1-D Cache Directory Sourced From Off Chip Off Book L3(E134) +
Count of Writes To L1-I Cache Directory Sourced From Off Book L4(E138) +
Count of Writes To L1-D Cache Directory Sourced From Off Book L4(E139) +

Sourced From Remote L4

–

Count of Writes To L1-I Cache Directory Sourced From On Book L4(E135) +
Count of Writes To L1-D Cache Directory Sourced From On Book L4(E136) +
Count of Writes To L1-I Cache Directory Sourced From Off Chip On Book L3(E152) +
Count of Writes To L1-D Cache Directory Sourced From Off Chip On Book L3(E155) +

Sourced From Local L4


LSPR TERMS

Relative Nest Intensity (RNI)

Indicates the level of activity to shared caches and memory

Calculating Relative Nest Intensity

The RNI of a workload may be calculated using CPU MF data. For z10, three factors are used:

- L2LP: percentage of L1 misses sourced from the local book L2 cache
- L2RP: percentage of L1 misses sourced from a remote book L2 cache
- MEMP: percentage of L1 misses sourced from memory.

These percentages are multiplied by weighting factors and the result divided by 100. The formula for z10 is:

z10 RNI=(1.0xL2LP+2.4xL2RP+7.5xMEMP)/100.

Tools available from IBM (zPCR) and several vendors can extract these factors from CPU MF data. For z196 the CPU MF factors needed are:

- L3P* percentage of L1 misses sourced from the shared chip-level L3 cache
- L4LP: percentage of L1 misses sourced from the local book L4 cache
- L4RP* percentage of L1 misses sourced from a remote book L4 cache
- MEMP: percentage of L1 misses sourced from memory

The formula for z196 is:

z196 RNI=1.6x(0.4xL3P+1.0xL4LP+2.4xL4RP+7.5xMEMP)/100

Note these formulas may change in the future.

LSPR Workload Categories

Please Send Your Data To IBM WSC. It will help everybody !!!

Knowledge Gain Is Still Evolving!

LSPR Workload Categories

Introduction

Historically, LSPR workload capacity curves (primitives and mixes) have had application names or been identified by a software characteristic. For example, past workload names have included CICS, IMS, OLTP-T, CB-L, LoIO-mix and TI-mix. However, capacity performance has always been more closely associated with how a workload uses and interacts with a particular processor hardware design. With the availability of CPU MF (SMF 113) data on z10, the ability to gain insight into the interaction of workload and hardware design in production workloads has arrived. The knowledge gained is still evolving, but the first step in the process is to produce LSPR workload capacity curves based on the underlying hardware sensitivities. Thus the LSPR introduces three new workload capacity categories which replace all prior primitives and mixes.

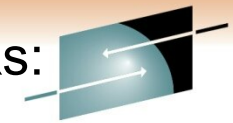
WORKLOAD CAPACITY PERFORMANCE IS SENSITIVE TO

Instruction Path Length For A Transaction Or Job

Instruction Complexity(Microprocessor Design)

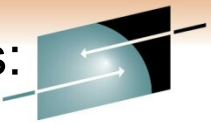
Memory Hierarchy Or Nest

Workload Capacity Performance is sensitive to 3 MAJOR FACTORs:



1. Instruction Path Length for a transaction or job
   - Application dependent, of course
   - Generally invariant across processor designs
   - But can be sensitive to Nway (due to MP effects such as locking, work queue searches, etc)
2. Instruction Complexity (Micro processor design)
   - Many design alternatives
     - Cycle time (GHz), instruction architecture, pipeline, superscalar, Out-Of-Order, branch prediction and more
   - Workload effect
     - May be different with each processor design
     - But once established for a workload on a processor, does not change very much

Workload Capacity Performance is sensitive to 3 MAJOR FACTORs:



3

- Memory Hierarchy or "nest"
  - Many design alternatives
    - cache (levels, size, private, shared, latency, MESI protocol), controller, data buses
  - Workload effect
    - Quite variable
    - Sensitive to many factors: locality of reference, dispatch rate, IO rate, competition with other applications and/or LPARs, and more
  - Relative Nest Intensity
    - Activity beyond private-on-chip cache(s) is the most sensitive area
    - Reflects activity distribution and latency to shared caches and memory
    - Level 1 cache miss percentage also important
    - Data for cacluation available from CPU MF (SMF 113) starting with z10

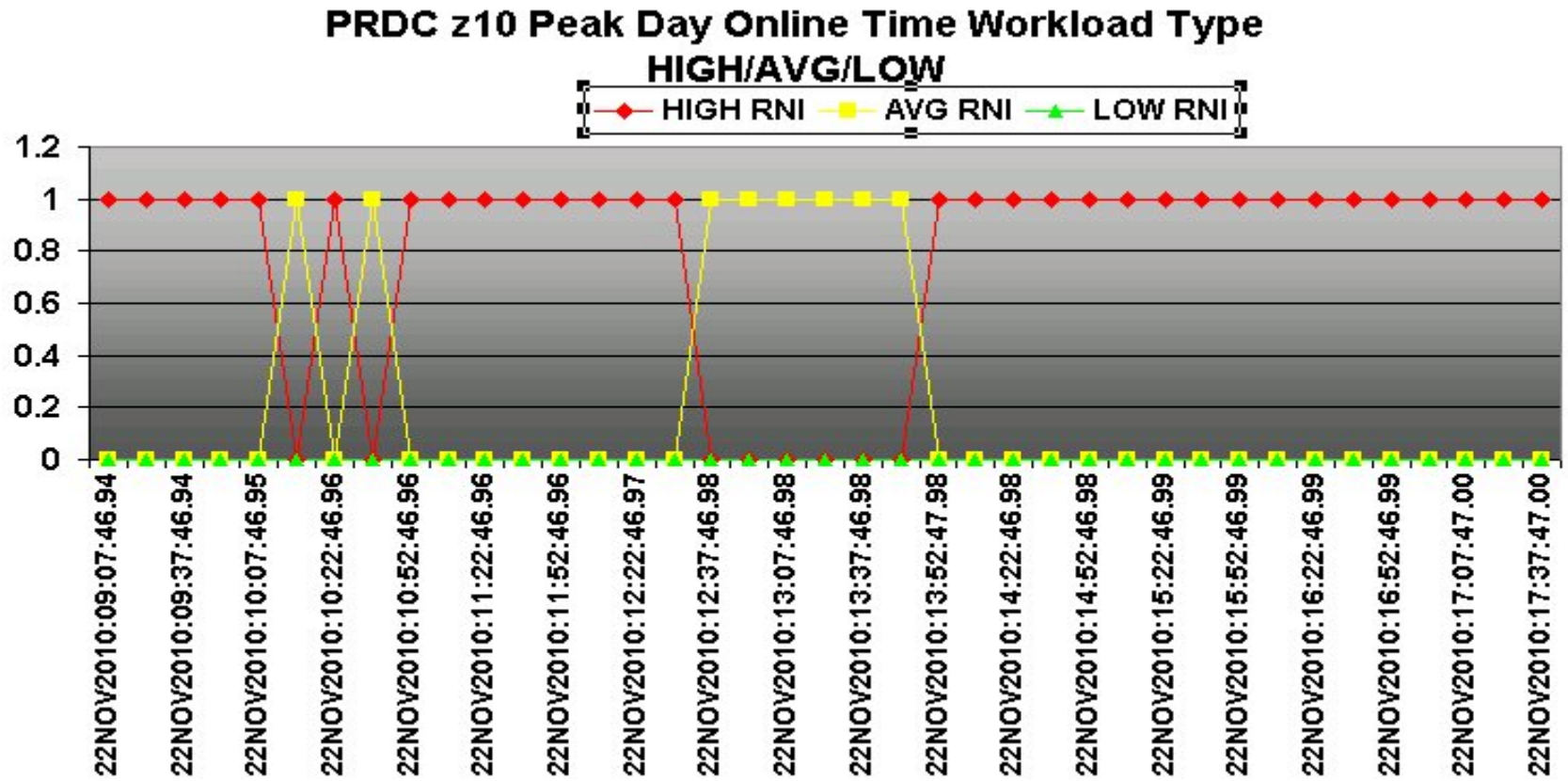
Workload Characterization

For z10 and newer processors, the CPU MF data may be used to provide an additional "hint" as to workload selection. When available, this data allows the RNI for a production workload to be calculated. Using the RNI and another value from CPU MF, the L1 cache miss percentage, a workload may be classified as LOW, AVERAGE or HIGH RNI. This classification and resulting "hint" is automated in the zPCR tool. It is highly recommended to use zPCR for capacity sizing. For those wanting to create the "hint" by hand, the following table may be used for z10:

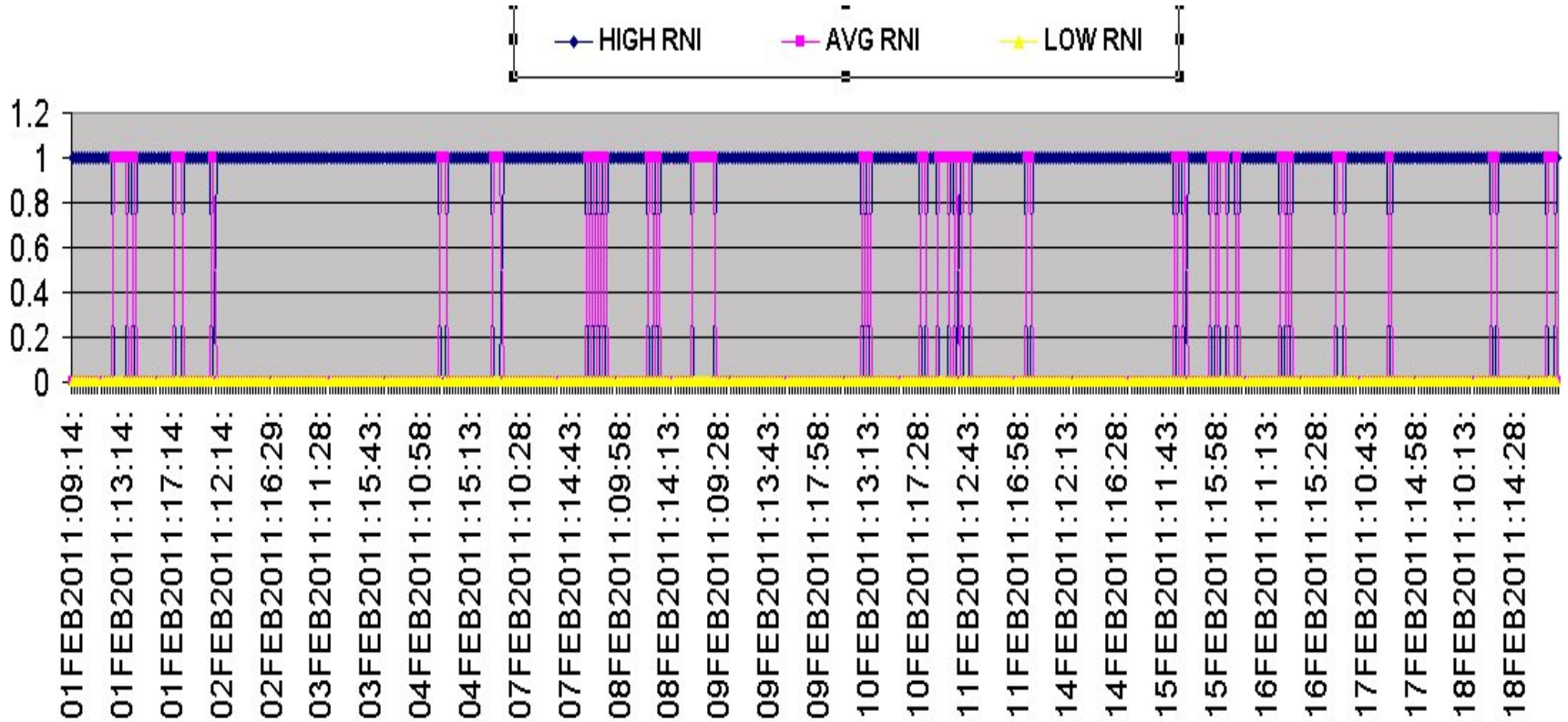
L1MP	RNI	Workload Hint
<3%	>= 0.75 < 0.75	AVERAGE LOW
3% to 6%	>1.0 0.6 to 1.0 < 0.6	HIGH AVERAGE LOW
>6%	>= 0.75 < 0.75	HIGH AVERAGE

Note this table may change in the future.

Sample Workload Type Changes During DayTime



Sample Workload Type Changes During Online Time Day –By-Day



Z10 To z196 Upgrade Performance Analiz Using SMF 113 Counters

Z10 To z196 – LPAR Weight Distribution

LPAR	z10 WEIGHT	z196 WEIGHT	z10 %- SHARE-WEIGHT	z196 %- SHAREWEIGTH
PRDA	161	18	9	10
PRDC	355	39	20	22
PRDE	979	109	56	60
PRDF	50	6	3	3
PRDB	381	42	23	23
PRDD	727	81	45	45
PRDG	375	42	23	23
PRDW	60	6	4	3

Z10- 722 MSU 1631
Z10-724 MSU 1748
Z196-717 MSU 1816

→ **> HALF OF THE CEC**

→ **NEARLY HALF OF THE CEC**

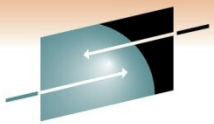
Z10 GAR1 Total Weight : 1631
Z10 GAR2 Total Weight : 1748

Z196 GAR1 Total Weight : 1816
Z196 GAR2 Total Weight : 1816

EACH 12 LOGICAL PROCESSOR DEFINED **IRD**

Other small LPARs : Prod & Test GDPS Controlling Systems & Test Systems

Z196 GAR1 CEC Actual PU Distribution



SHARE
Technology · Connections · Results

ERM config CPU=17 SAP=6 ICF=2 IFL=0 zAAP=0 zIIP=2 SP=13 UKNW=0 OP=27 XSTP=0 z196 2817

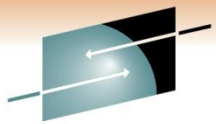
Node Number(Phy)	01	01		01	01	01	01	01		01	01	01	01		01	01	01	01	01	01		01	01	01
Core Number	00	00		00	01	01	01	01		02	02	02	03		03	03	04	04	04	04		05	05	05
IPU Number	17	11		16	03	04	05	06		07	08	09	0A		0B	0C	01	0E	0F	10		00	12	2F
Physical PU Number	100	101		103	104	105	106	107		109	10A	10B	10C		10E	10F	110	111	112	113		115	116	117
PU Number	17	00		16	03	04	05	06		07	08	09	0A		0B	01	01	0E	0F	02		00	12	00
Opertional Mode CPU					03	04	05	06		07	08	09	0A		0B		01	0E	0F			00	12	
ICF																								
SAP																								
MSAP																01				02				
XSAP																								00
IFL																								
zAAP																								
zIIP	17			16																				
Spare		00																						
Unknown PU Type																								
Dedicate																								
Opertional	Y			Y	Y	Y	Y	Y		Y	Y	Y	Y		Y	Y	Y	Y	Y	Y		Y	Y	Y
Clock Stopped																								

Book01 14 CPU 2 zIIPs 3 SAPs

Node Number(Phy)		03	03	03	03	03	03	03	03	03	03		03		03	03	03	03	03	03		03	03	03
Core Number		00	00	00	01	01	01	01	02	02	02		03		03	03	04	04	04	04		05	05	05
IPU Number		20	14	15	21	22	18	19	1A	1B	1C		1D		1E	1F	13	02	0D	23		24	25	26
Physical PU Number		301	302	303	304	305	306	307	308	309	30A		30C		30E	30F	310	311	312	313		315	316	317
PU Number		00	14	15	00	00	00	00	00	00	00		00		00	03	13	02	0D	04		00	00	05
Opertional Mode CPU																	13	02	0D					
ICF			14	15																				
SAP																								
MSAP																03				04				05
XSAP																								
IFL																								
zAAP																								
zIIP																								
Spare		00			00	00	00	00	00	00	00		00		00							00	00	
Unknown PU Type																								
Dedicate			Y	Y																				
Opertional			Y	Y												Y	Y	Y	Y	Y				Y
Clock Stopped																								

Book03 3 CPU 2 ICFs 3 SAPs

Z196 GAR2 CEC Actual PU Distribution



ERM config CPU=17 SAP=6 ICF=2 IFL=0 zAAP=0 zIIP=1 SP=14 UKNW=0 OP=26 XSTP=0 z196 2817

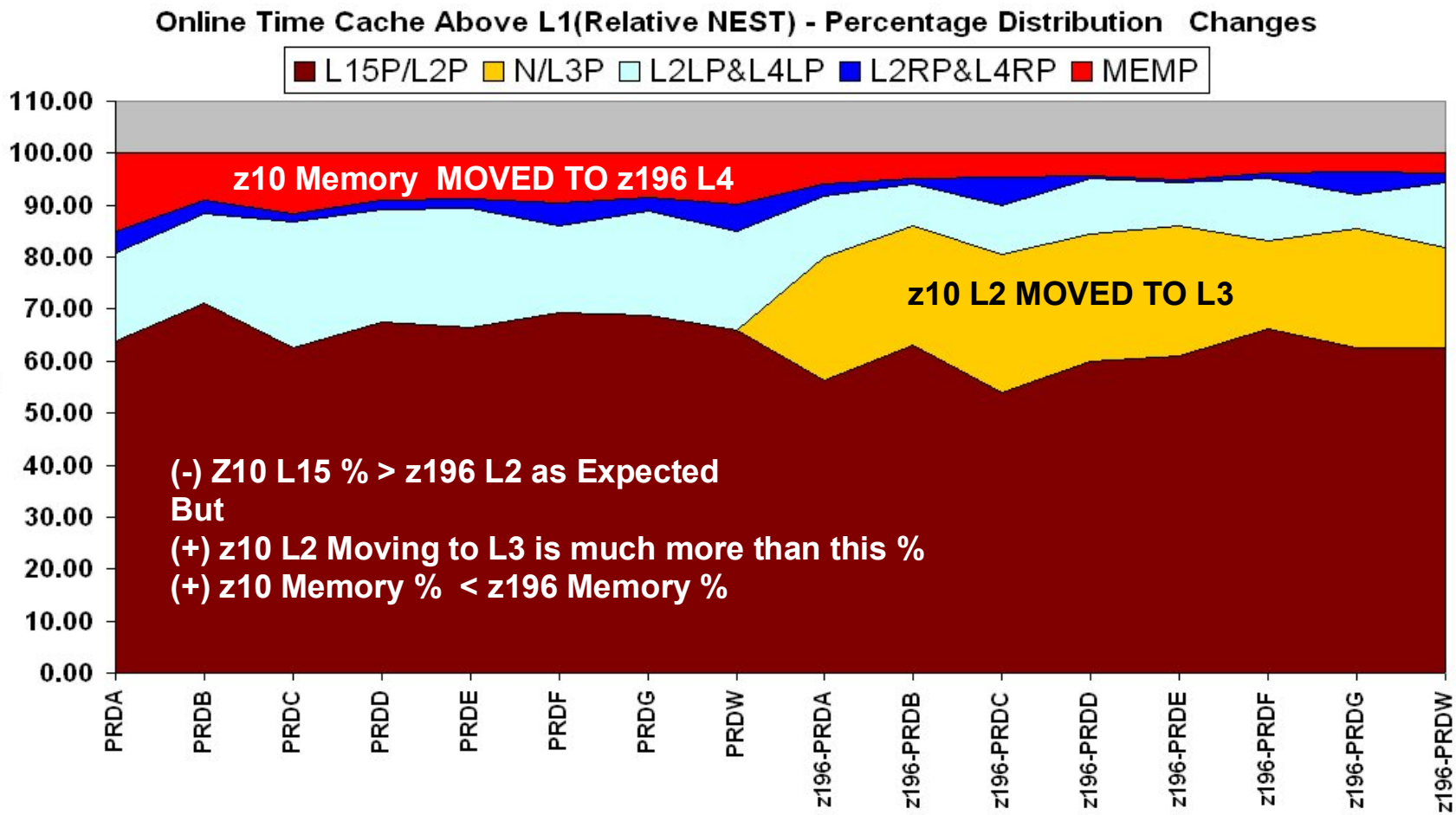
Node Number(Phy)		01	01	01	01	01	01	01	01		01	01	01		01	01	01	01	01	01	01		01	01
Core Number		00	00	00	01	01	01	01	02		02	02	03		03	03	04	04	04	04	05		05	05
IPU Number		0A	16	11	01	04	05	06	07		08	09	02		0B	0C	0D	0E	0F	10	00		12	2F
Physical PU Number		101	102	103	104	105	106	107	108		10A	10B	10C		10E	10F	110	111	112	113	114		116	117
PU Number		0A	16	00	01	04	05	06	07		08	09	02		0B	01	0D	0E	0F	02	00		12	00
Opertional Mode CPU		0A			01	04	05	06	07		08	09	02		0B		0D	0E	0F		00		12	
ICF																								
SAP																								
MSAP																01				02				
XSAP																								00
IFL																								
zAAP																								
zIIP			16																					
Spare				00																				
Unknown PU Type																								
Dedicate																								
Opertional		Y	Y		Y	Y	Y	Y	Y		Y	Y	Y		Y	Y	Y	Y	Y	Y	Y		Y	Y
Clock Stopped																								

Book01 15 CPU 1 zIIP 3 SAPs

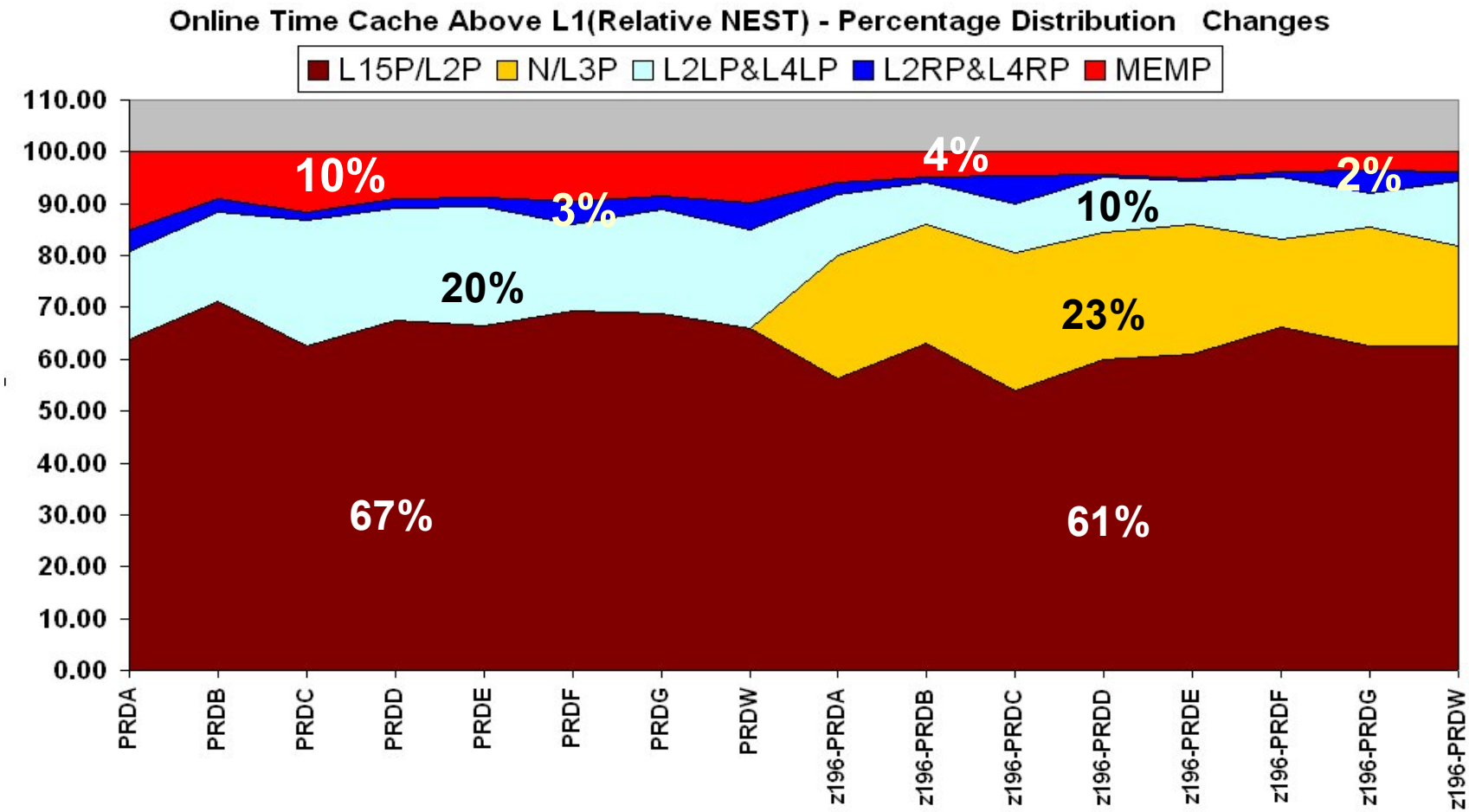
Node Number(Phy)	03	03	03		03	03	03	03		03	03	03	03		03	03	03	03	03	03	03		03	03
Core Number	00	00	00		01	01	01	01		02	02	02	03		03	03	04	04	04	04	05		05	05
IPU Number	24	14	15		25	17	18	19		1A	1B	1C	1D		1E	1F	20	21	22	23	13		03	26
Physical PU Number	300	301	302		304	305	306	307		309	30A	30B	30C		30E	30F	310	311	312	313	314		316	317
PU Number	00	14	15		00	00	00	00		00	00	00	00		00	03	00	00	00	04	13		03	05
Opertional Mode CPU																					13		03	
ICF		14	15																					
SAP																								
MSAP																03				04				05
XSAP																								
IFL																								
zAAP																								
zIIP																								
Spare	00				00	00	00	00		00	00	00	00		00		00	00	00					
Unknown PU Type																								
Dedicate		Y	Y																					
Opertional		Y	Y													Y				Y	Y		Y	Y
Clock Stopped																								

Book03 2 CPU 2 ICFs 3 SAPs

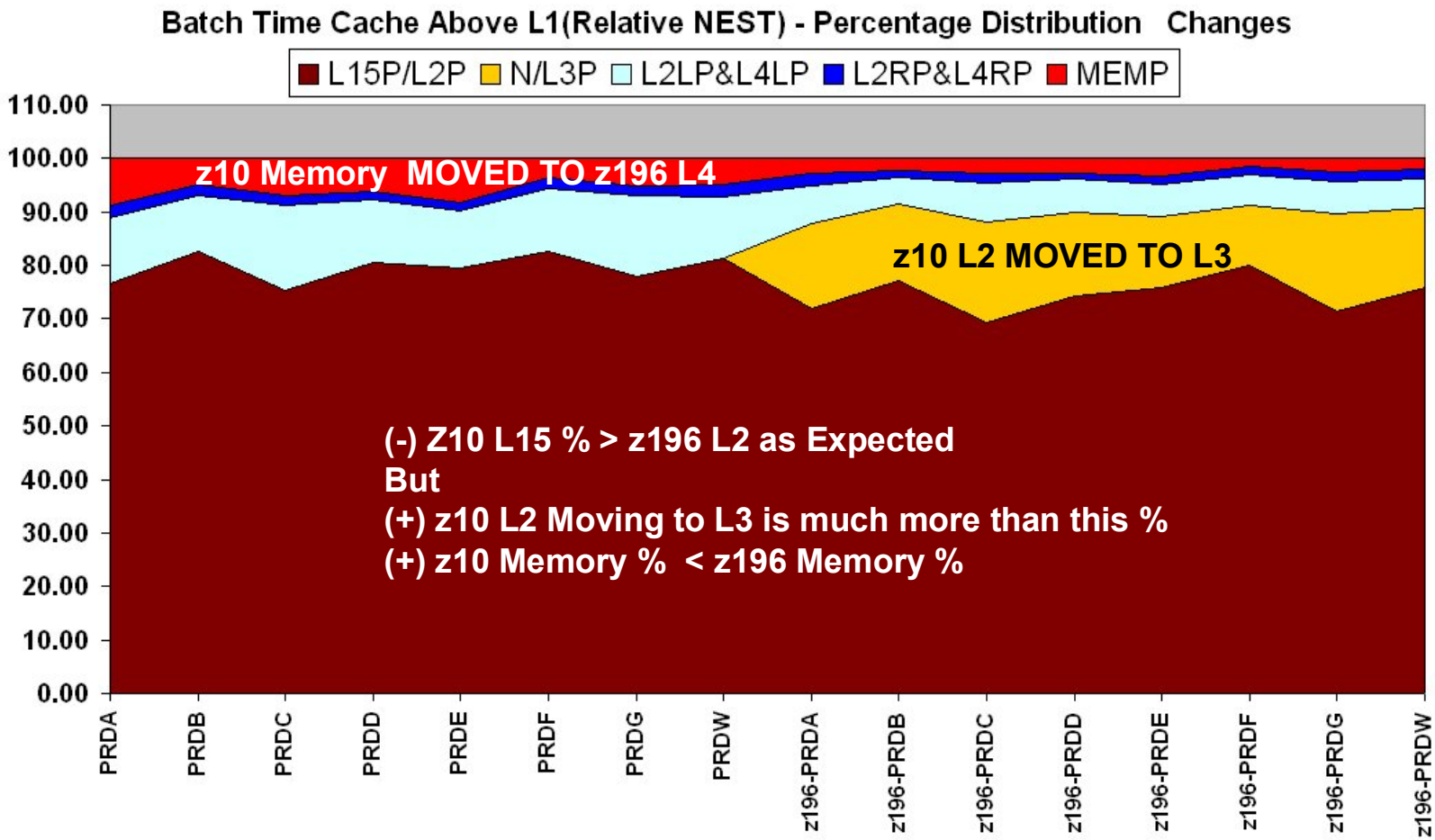
z10 & z196 Online Period - CACHE SOURCED DISTRIBUTION



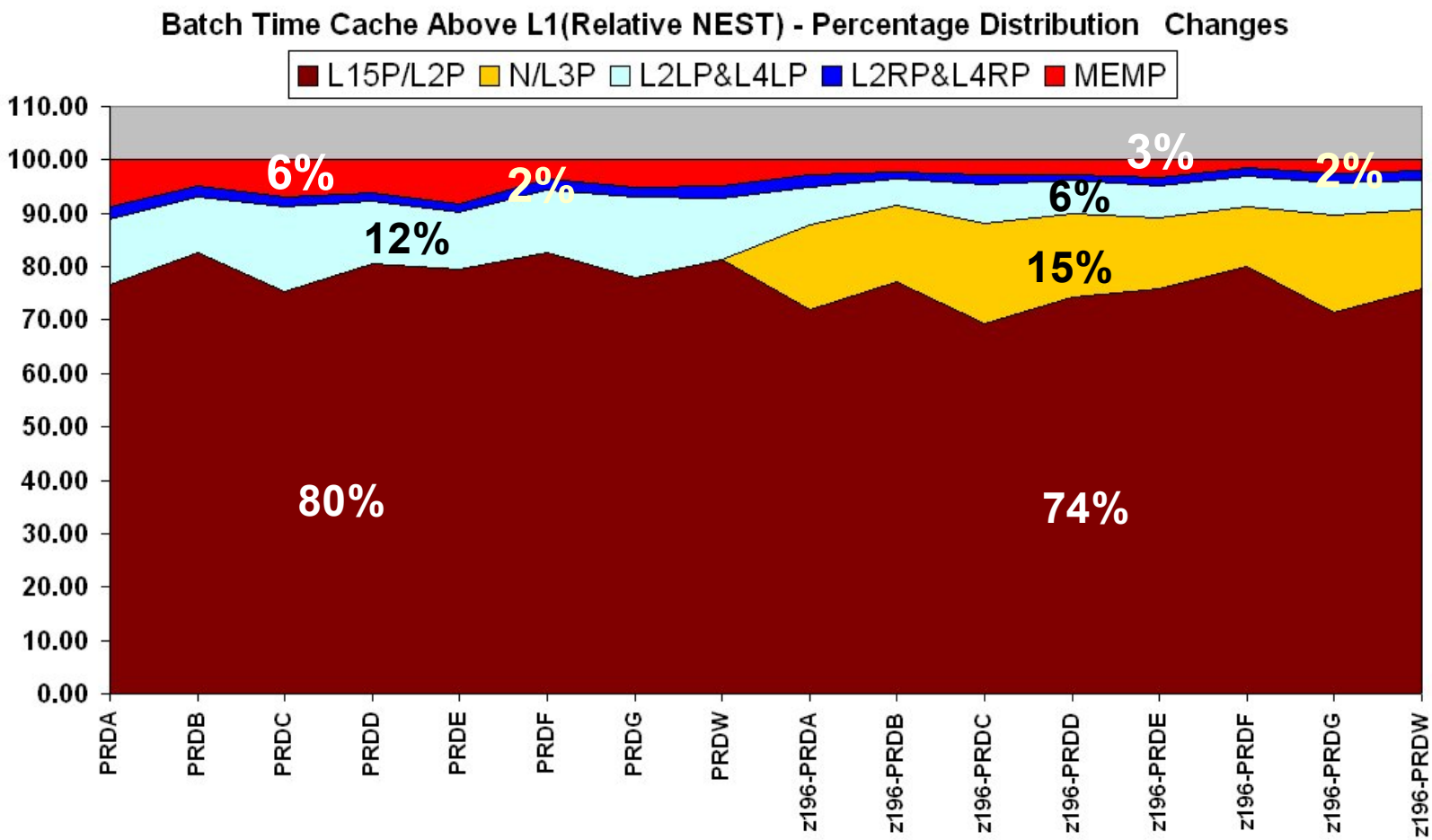
z10 & z196 Online Period - CACHE SOURCED DISTRIBUTION



z10 & z196 Batch Period - CACHE SOURCED DISTRIBUTION

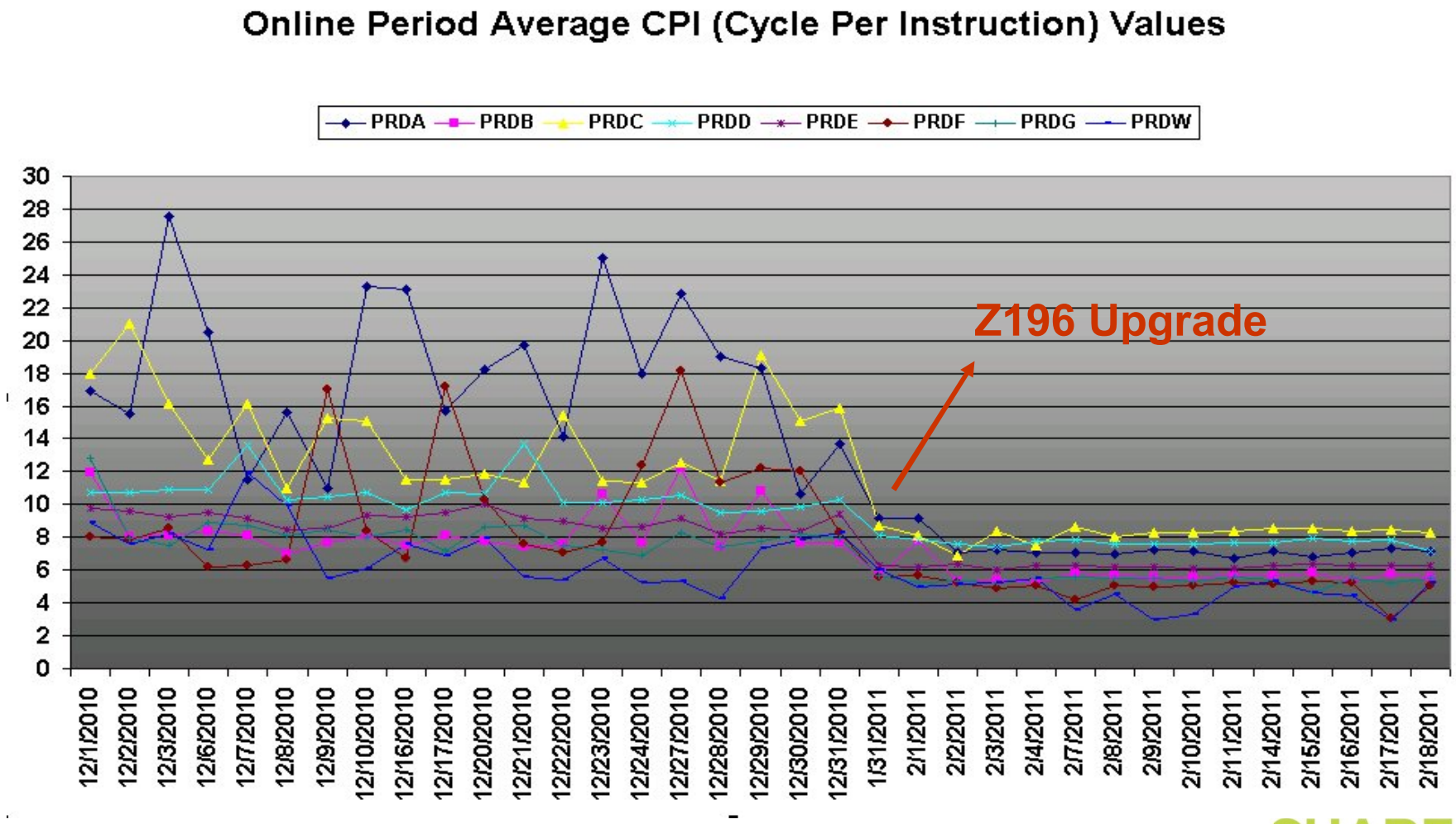


z10 & z196 Batch Period - CACHE SOURCED DISTRIBUTION



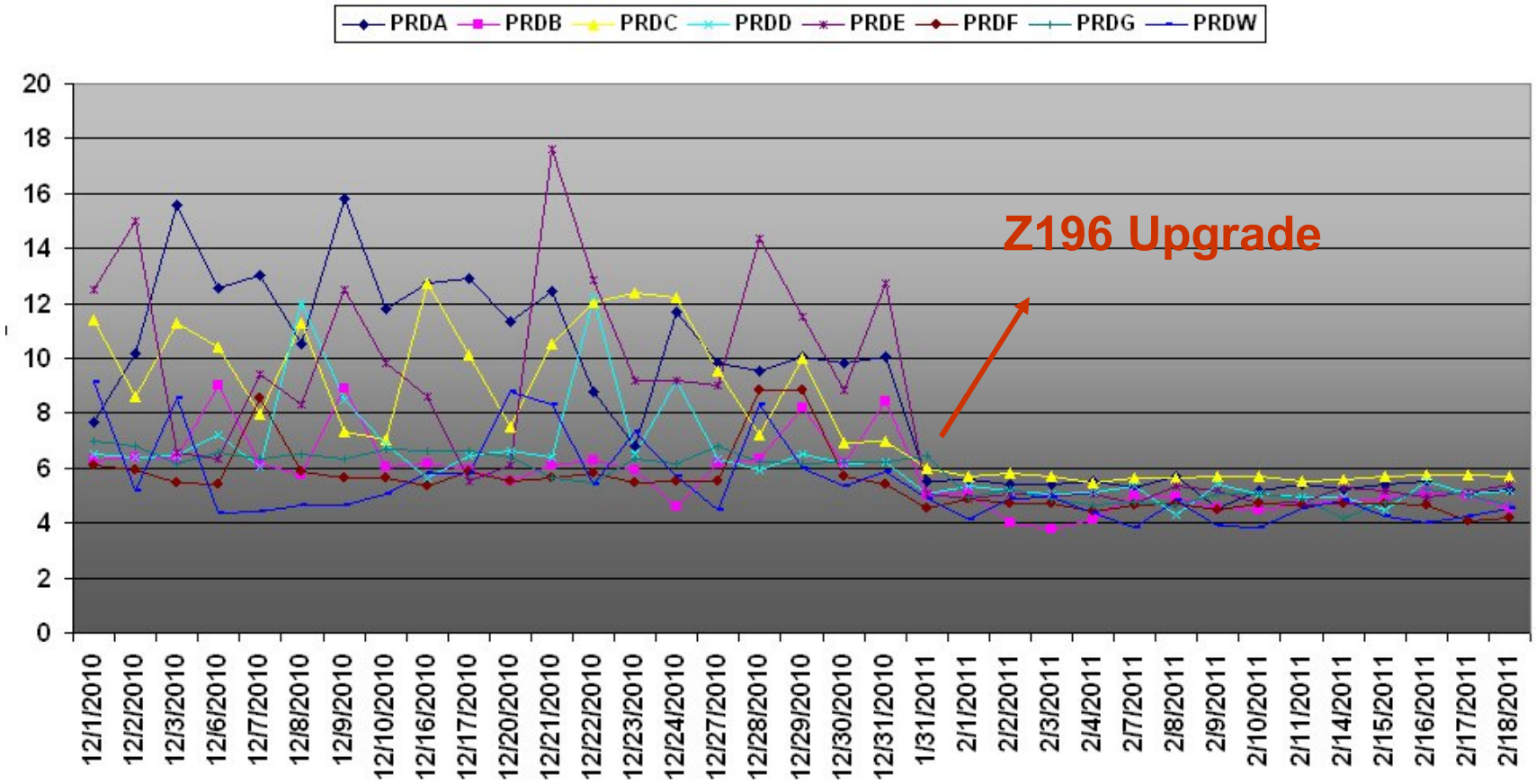
CPI- Online

Online Period : December and February All Days Except Weekends 08<HOUR<18 :



CPI- Batch

Batch Period : December and February All Days Except Weekends 08<HOUR<18 :

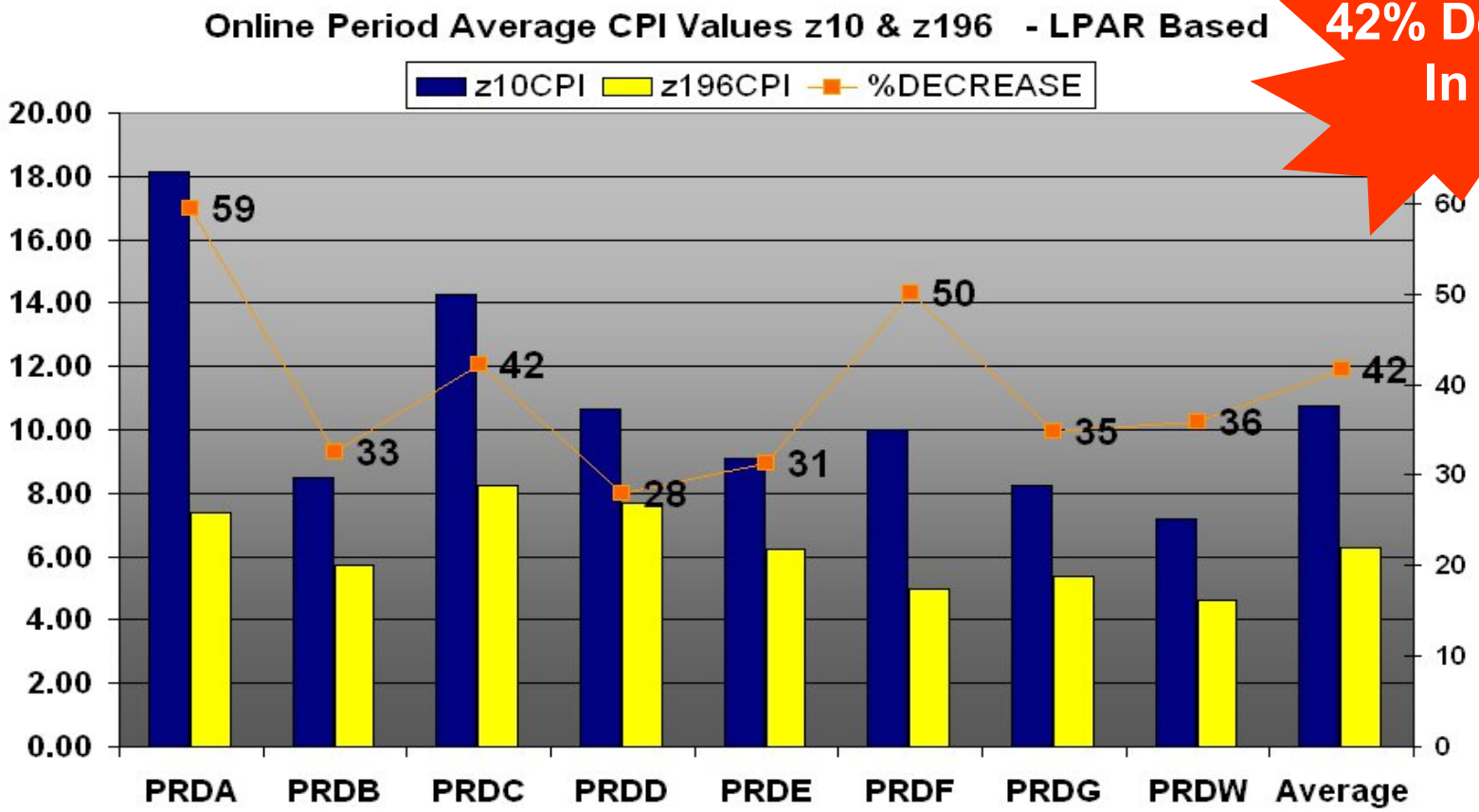


Workload Type Difference Between Batch & Online Period

BATCH				ONLINE			
SYSTEM	z10CPI	z196CPI	%Decrease	SYSTEM	z10CPI	z196CPI	%Decrease
PRDA	11.2	5.3	52.3	PRDA	18.1	7.4	59.4
PRDB	6.5	4.7	28.6	PRDB	8.5	5.7	32.6
PRDC	9.7	5.7	41.3	PRDC	14.3	8.2	42.3
PRDD	7.2	5.1	29.8	PRDD	10.7	7.7	28.0
PRDE	10.4	5.0	51.4	PRDE	9.1	6.2	31.3
PRDF	6.1	4.6	25.0	PRDF	10.0	5.0	50.0
PRDG	6.4	5.0	21.9	PRDG	8.2	5.4	34.8
PRDW	6.2	4.4	28.7	PRDW	7.2	4.6	35.8
Average	8.0	5.0	37.5	Average	10.8	6.3	41.6

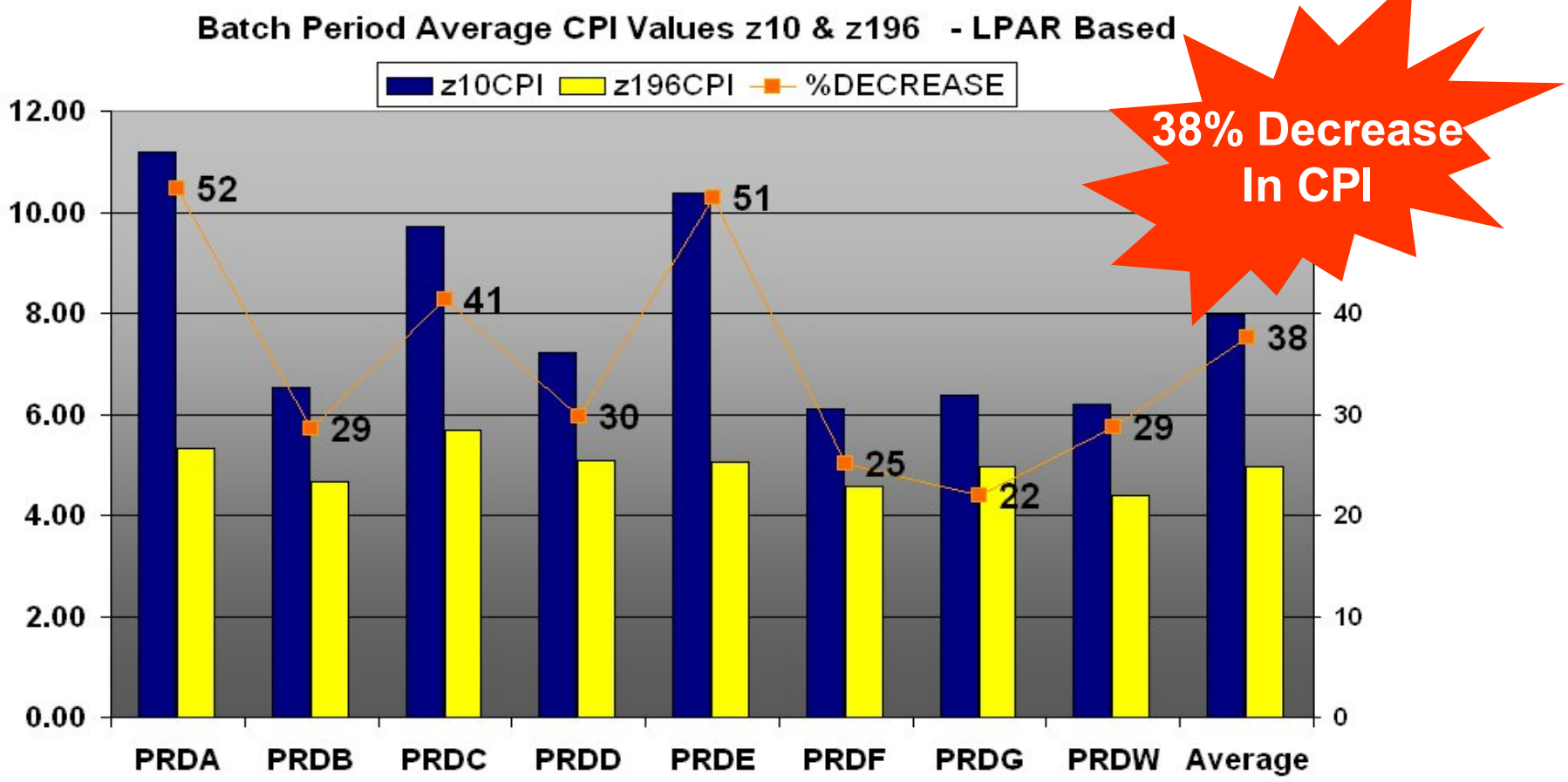
Workload Type Difference Between Batch & Online Period

- BIG LPARs effected less than small LPARs
- Small LPARs have higher CPI values



42% Decrease In CPI

Workload Type Difference Between Batch & Online Period



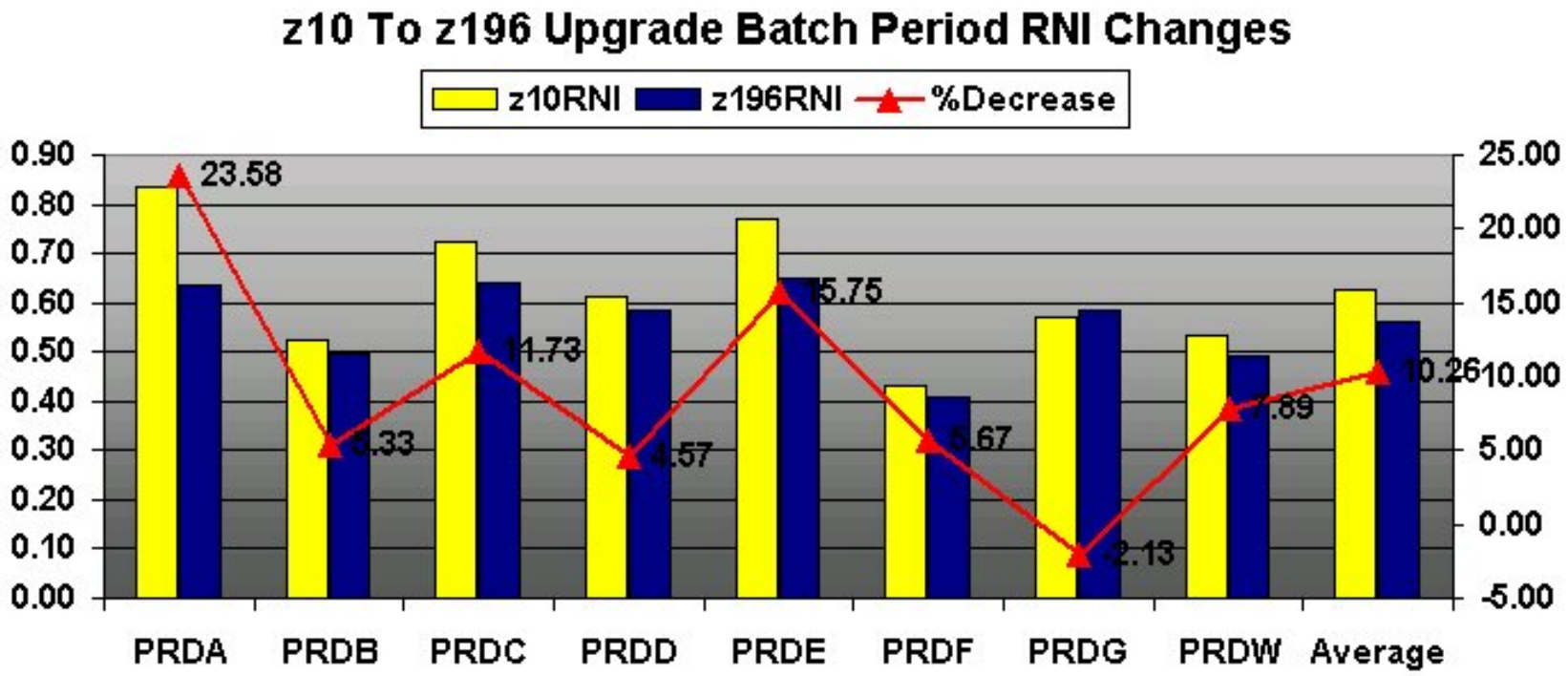
Workload Type Difference Between Batch & Online Period

- Batch Period Is Much More CPU Sensitive Then Online Period OR
- Online Period Is Much More Data Intensive(Cache Miss) Then Batch Period

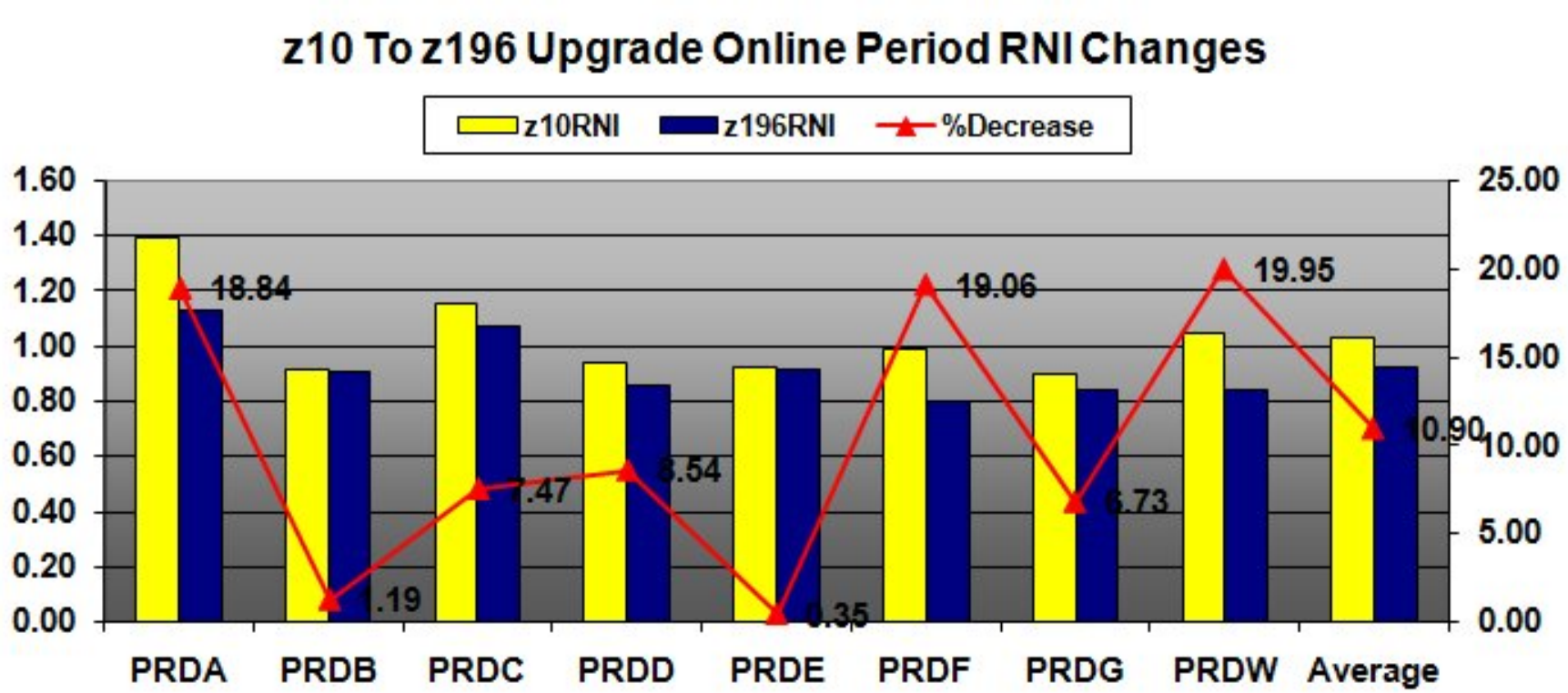
BATCH				ONLINE			
SYSTEM	z10RNI	z196RNI	%Decrease	SYSTEM	z10RNI	z196RNI	%Decrease
PRDA	0.83	0.64	23.58	PRDA	1.39	1.13	18.84
PRDB	0.53	0.50	5.33	PRDB	0.92	0.91	1.19
PRDC	0.73	0.64	11.73	PRDC	1.16	1.07	7.47
PRDD	0.61	0.58	4.57	PRDD	0.94	0.86	8.54
PRDE	0.77	0.65	15.75	PRDE	0.92	0.92	0.35
PRDF	0.43	0.41	5.67	PRDF	0.99	0.80	19.06
PRDG	0.57	0.59	-2.13	PRDG	0.90	0.84	6.73
PRDW	0.53	0.49	7.89	PRDW	1.05	0.84	19.95
Average	0.63	0.56	10.26	Average	1.03	0.92	10.90

Workload Type Difference Between Batch & Online Period

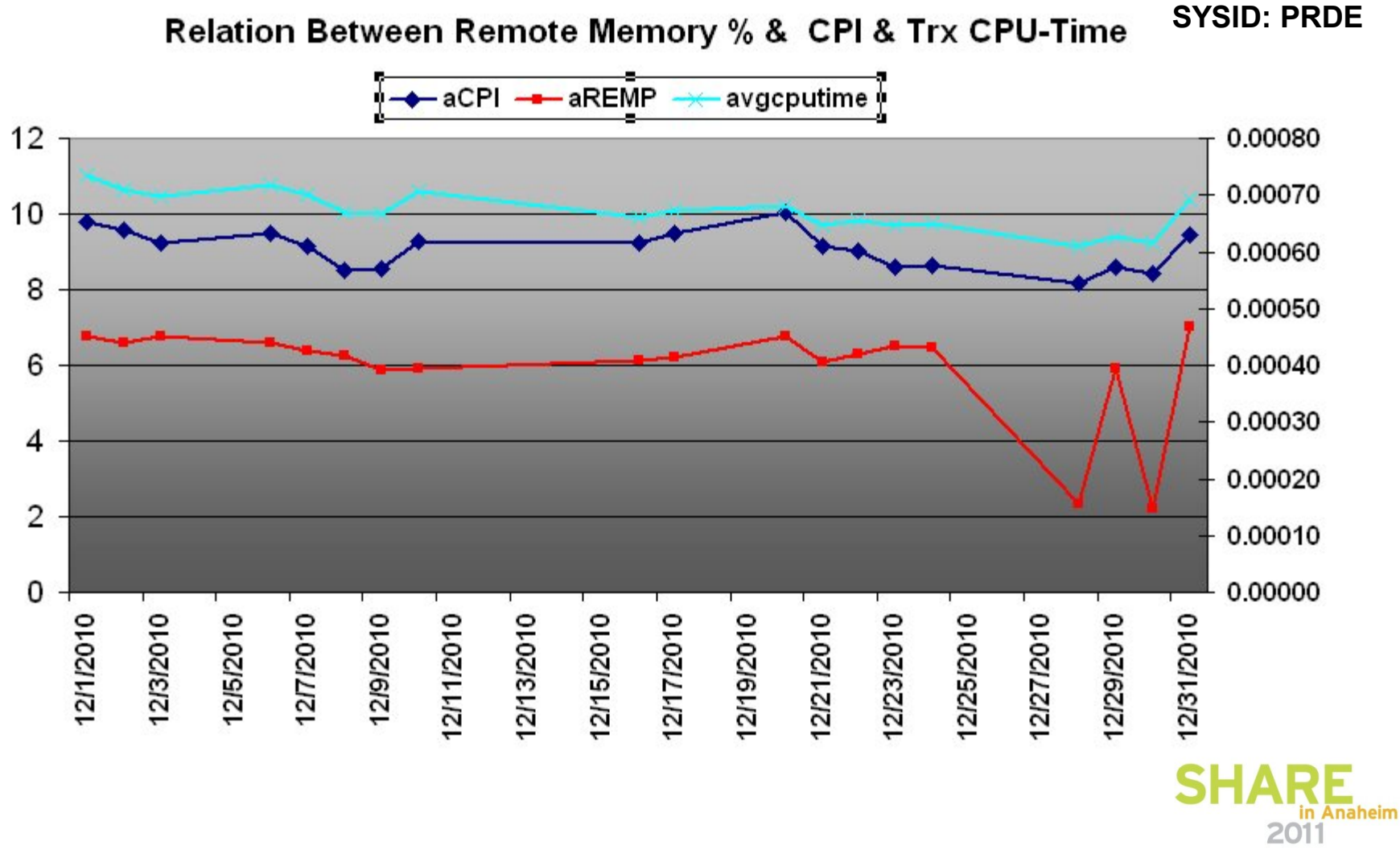
IBM s expection is to have same or lower RNI values when customers move to z196s.
The coefficients aim is to make equal RNI values between z10 and z196s



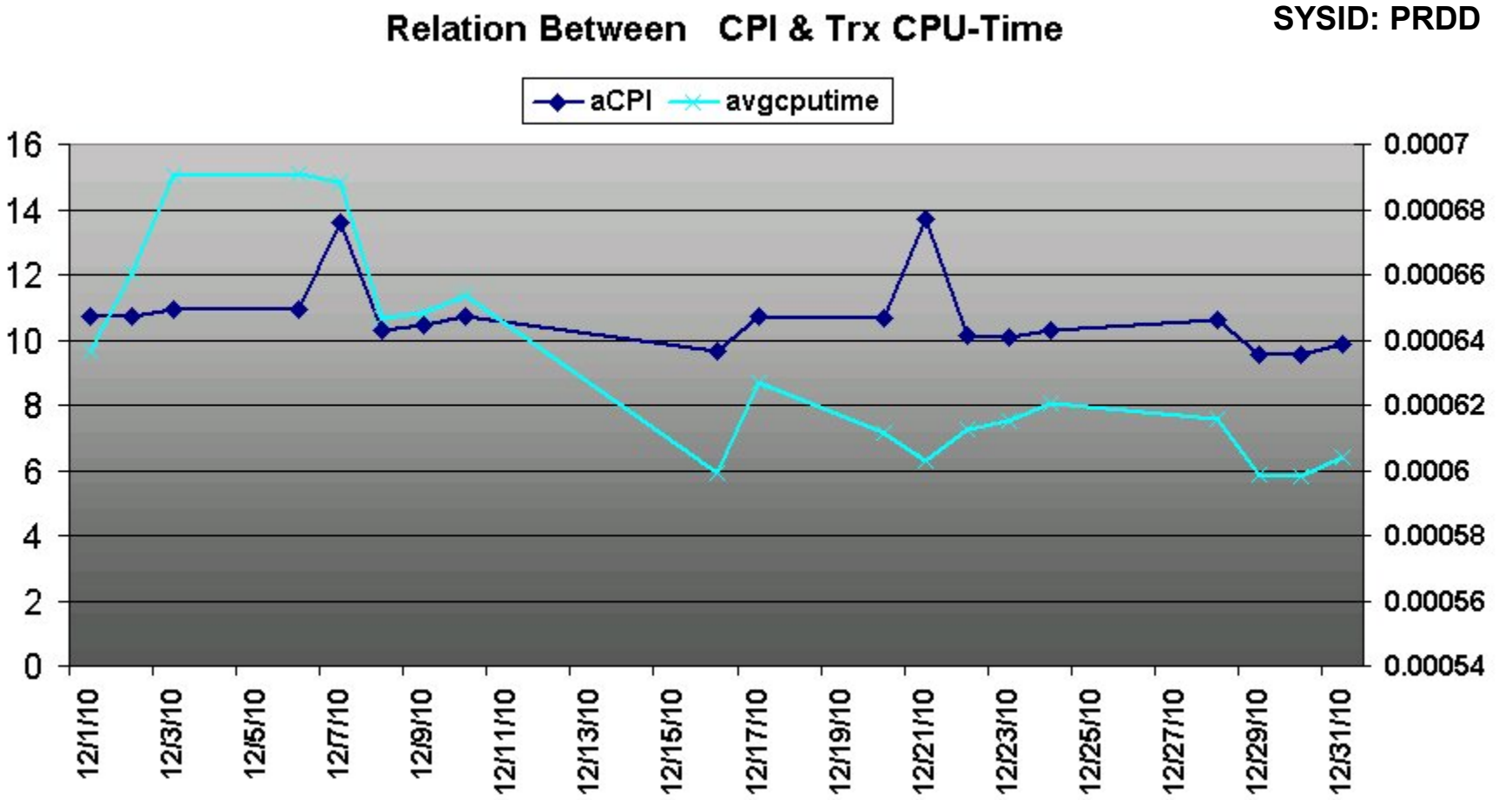
Workload Type Difference Between Batch & Online Period



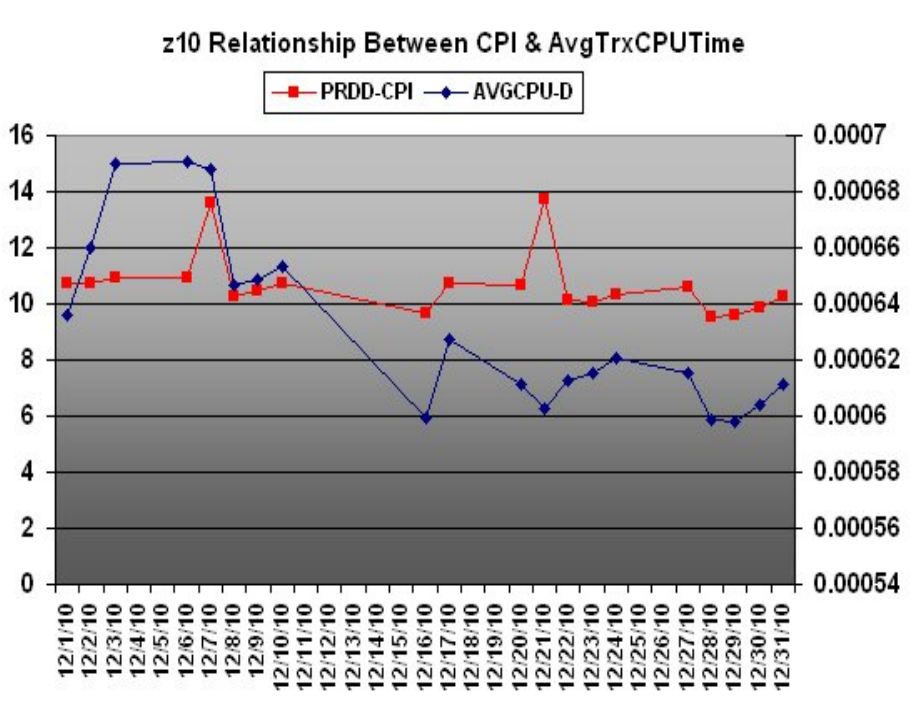
Relationship Between CPI & RemoteMemory & Average CPU Time of Trx

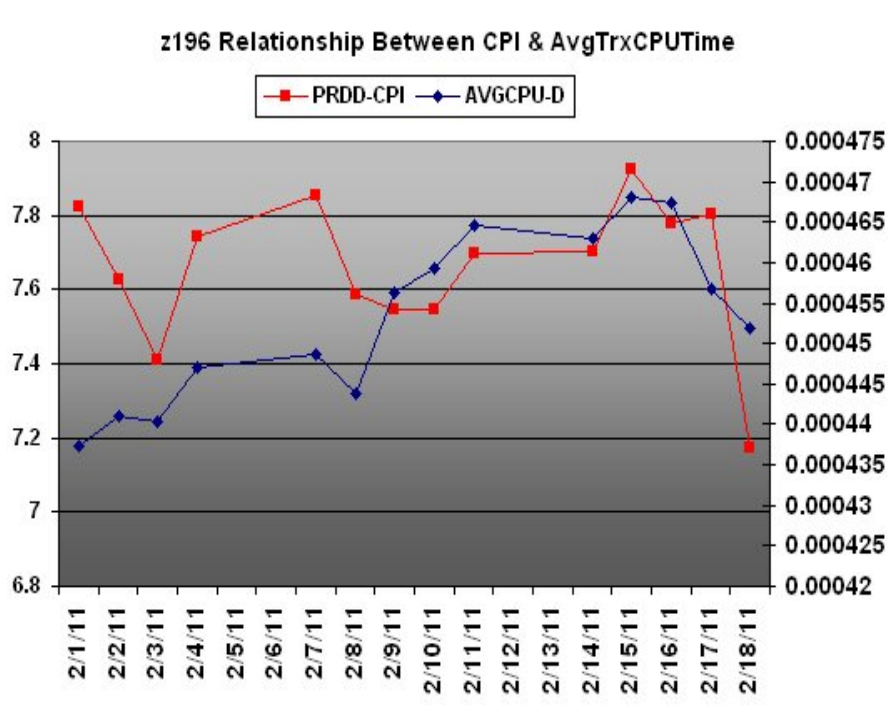


Relationship Between CPI & RemoteMemory & Average CPU Time of Trx

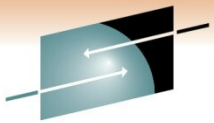


Relationship Between CPI & Average CPU Time of Trx





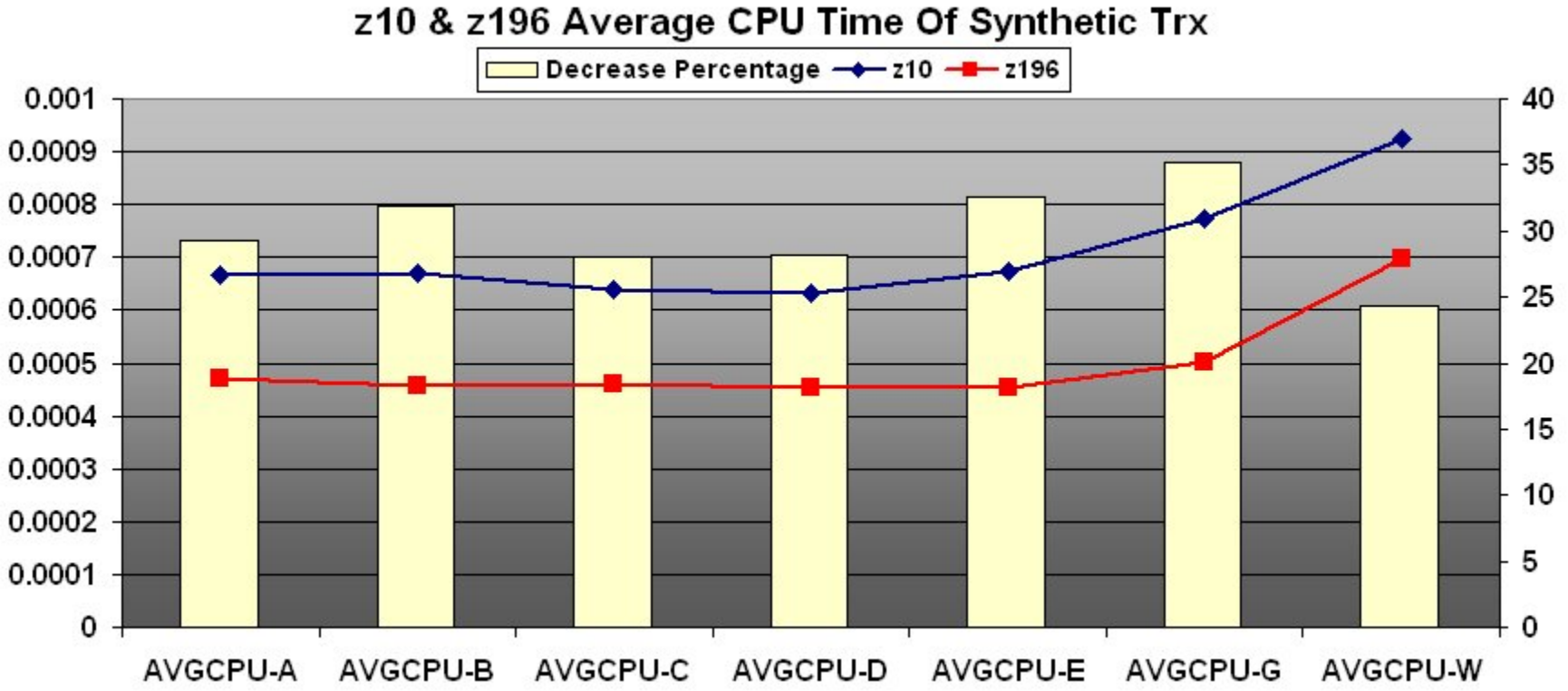
Z10 To z196 Upgrade- Syntetic Trx Avg Cpu Time Changes



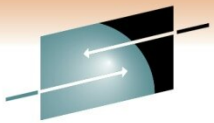
Z10 Online Time Synthetic Trx Avg CpuTime 0.00071

30% Decrease

Z196 Online Time Synthetic Trx Avg CpuTime 0.00049



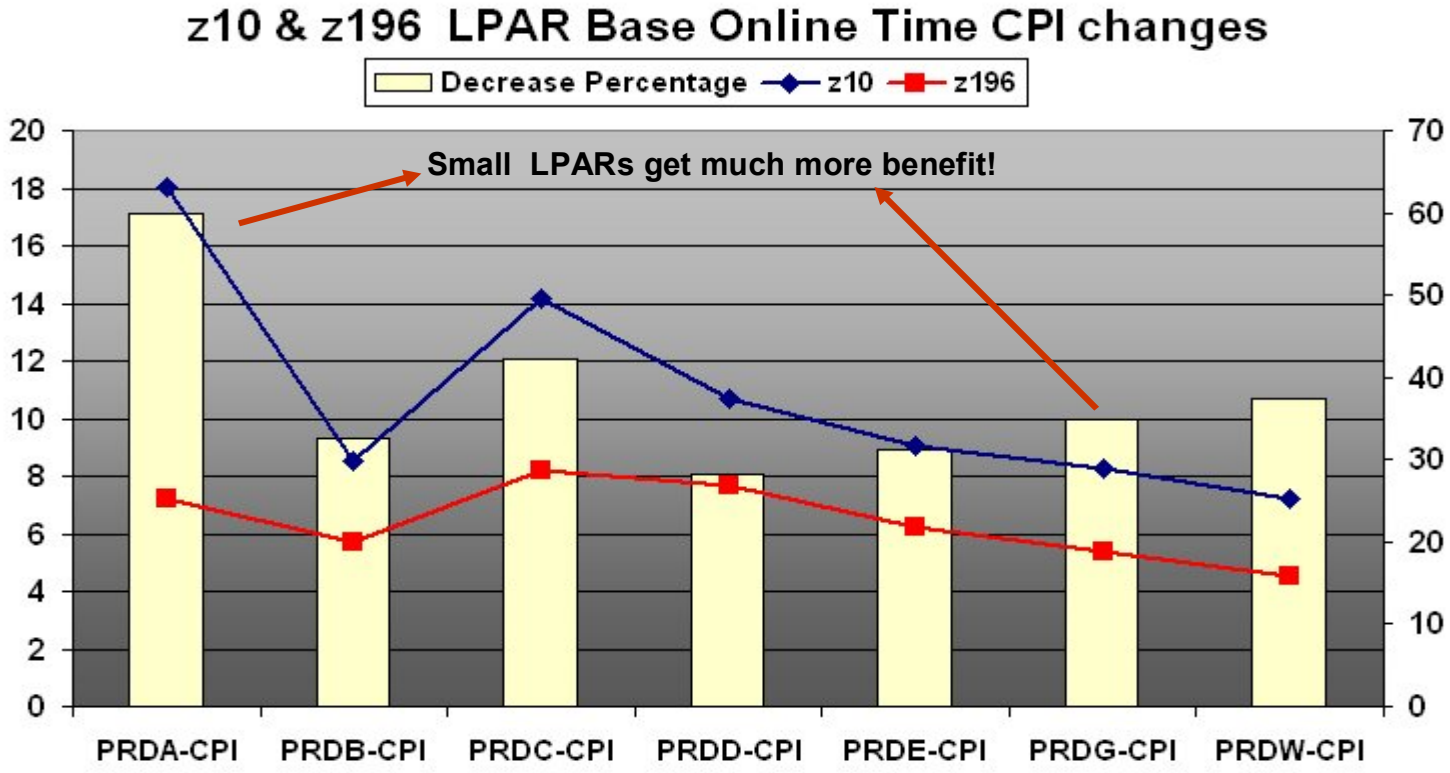
Z10 To z196 Upgrade- LPAR Base Online Time CPI Changes



Z10 Online Time LPAR Average CPI = 10.8

41% Decrease

Z196 Online Time LPAR Average CPI = 6.4

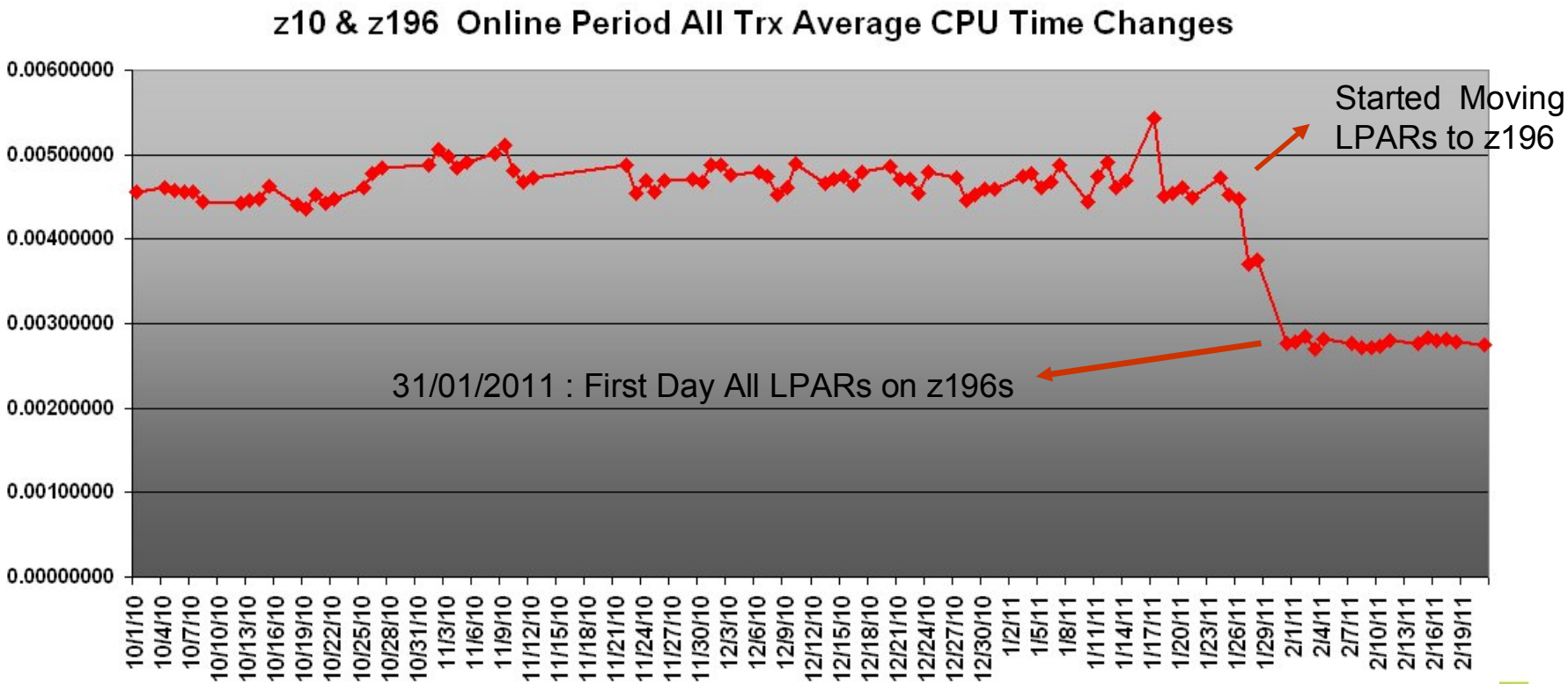


Z10 To z196 – Online Period All Trx Average CPU Time

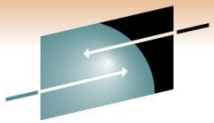
Z10 Online Time ALL Trx Avg CpuTime 0.0047

41% Decrease

Z196 Online Time ALL Trx Avg CpuTime 0.0027



Z10 To z196 – Online Workload View



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If we include trx count in batch period as well : Our Record Day Is 31/01/2011
236.698.209 Transaction In Average 0.0453 second Response Time

	Tarih	Toplam TRX	Ortalama Yanıt Süresi(sn)	Toplam CPU ss:dd:nn
TRX Sayısının En fazla Olduğu Gün :	31/01/2011	**236,698,209**	0.0453	183:56:59
CPU Kullanımın En fazla Olduğu Gün :	22/11/2010	233,446,429	0.0817	**210:02:26**

Tarih	Toplam TRX	Ortalama Yanıt Süresi(sn)	Toplam CPU ss:dd:nn
11/02/2011	194,477,108	0.0380	151:10:38
10/02/2011	189,232,822	0.0374	146:06:51
09/02/2011	190,611,627	0.0369	146:19:46
08/02/2011	199,791,141	0.0384	153:24:04
07/02/2011	224,475,711	0.0372	175:15:37
06/02/2011	71,241,056	0.0430	44:17:25
05/02/2011	95,935,129	0.0454	59:44:24
04/02/2011	200,778,982	0.0357	156:28:02
03/02/2011	187,955,754	0.0394	143:57:25
02/02/2011	194,113,179	0.0498	157:29:06
01/02/2011	210,613,909	0.0392	165:07:38
31/01/2011	**236,698,209**	0.0453	183:03:46
30/01/2011	62,238,725	0.0483	38:57:59
29/01/2011	82,439,929	0.0455	43:23:42
28/01/2011	199,704,296	0.0421	165:58:56
27/01/2011	192,309,556	0.0411	158:54:31
26/01/2011	204,691,316	0.0641	167:15:30
25/01/2011	195,210,611	0.0422	162:32:08
24/01/2011	205,738,639	0.0434	177:51:16

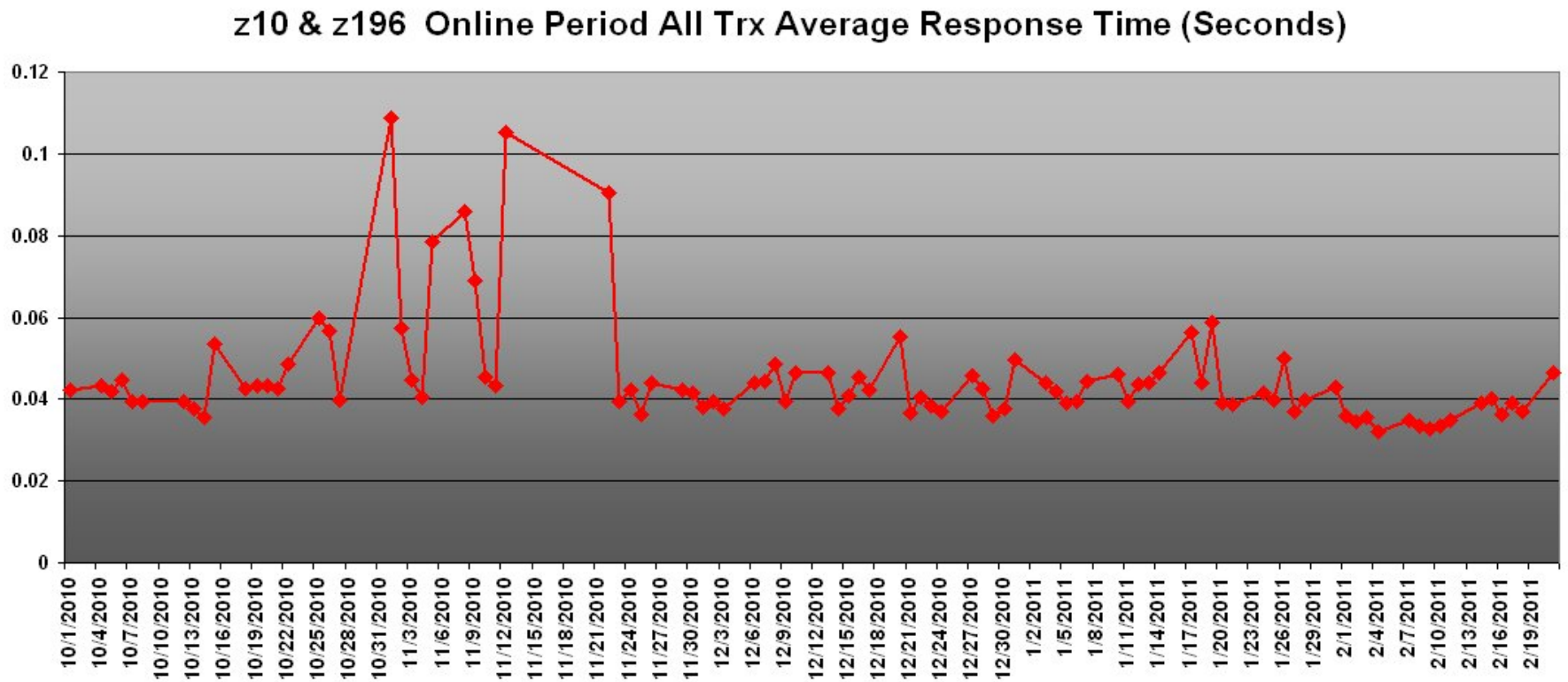
Normalized CPU Time

Z10 To z196 – Online Workload View

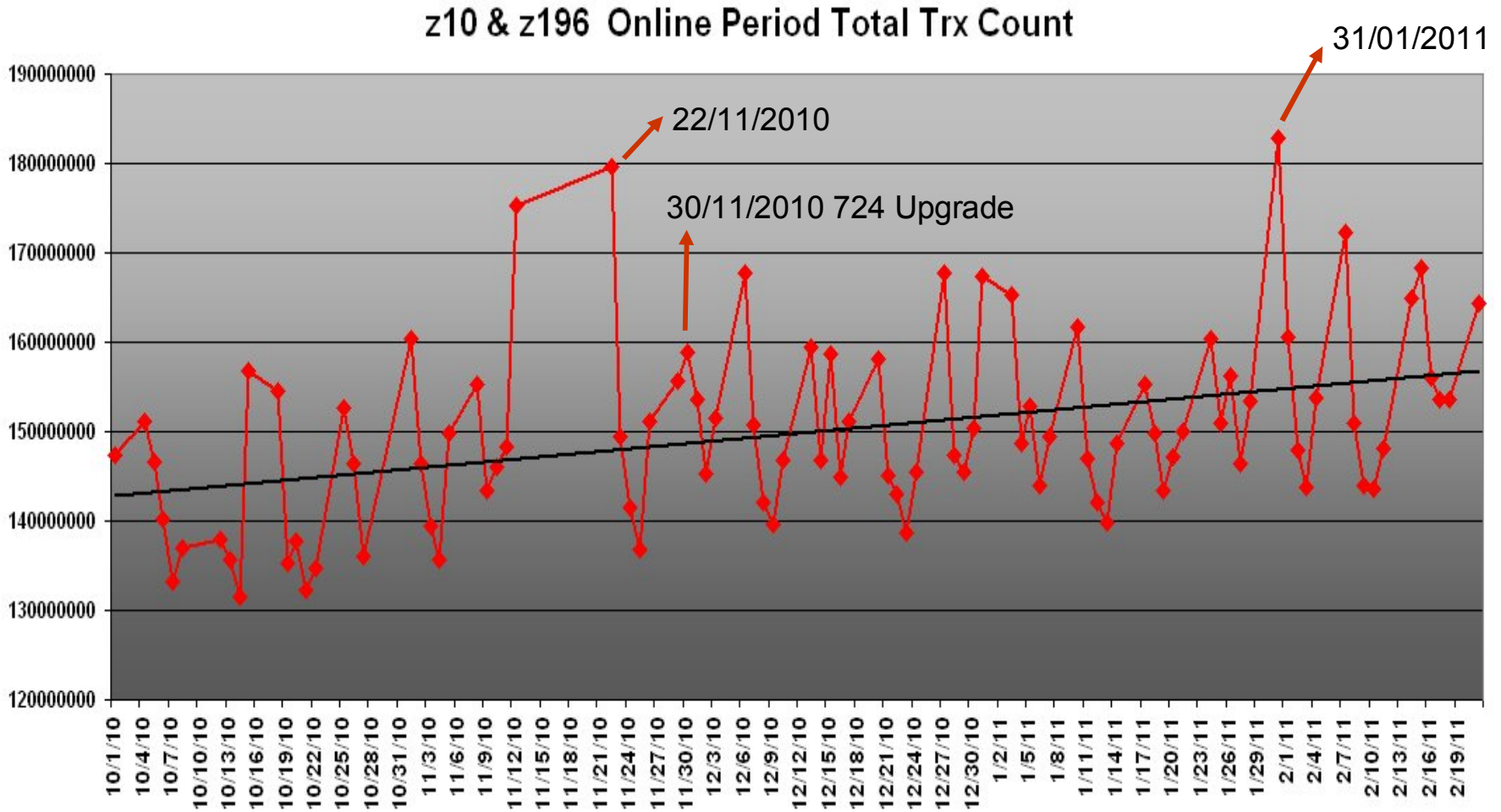
Z10 Online Time ALL Trx Avg ResponseTime 0.0042

14.5% Decrease

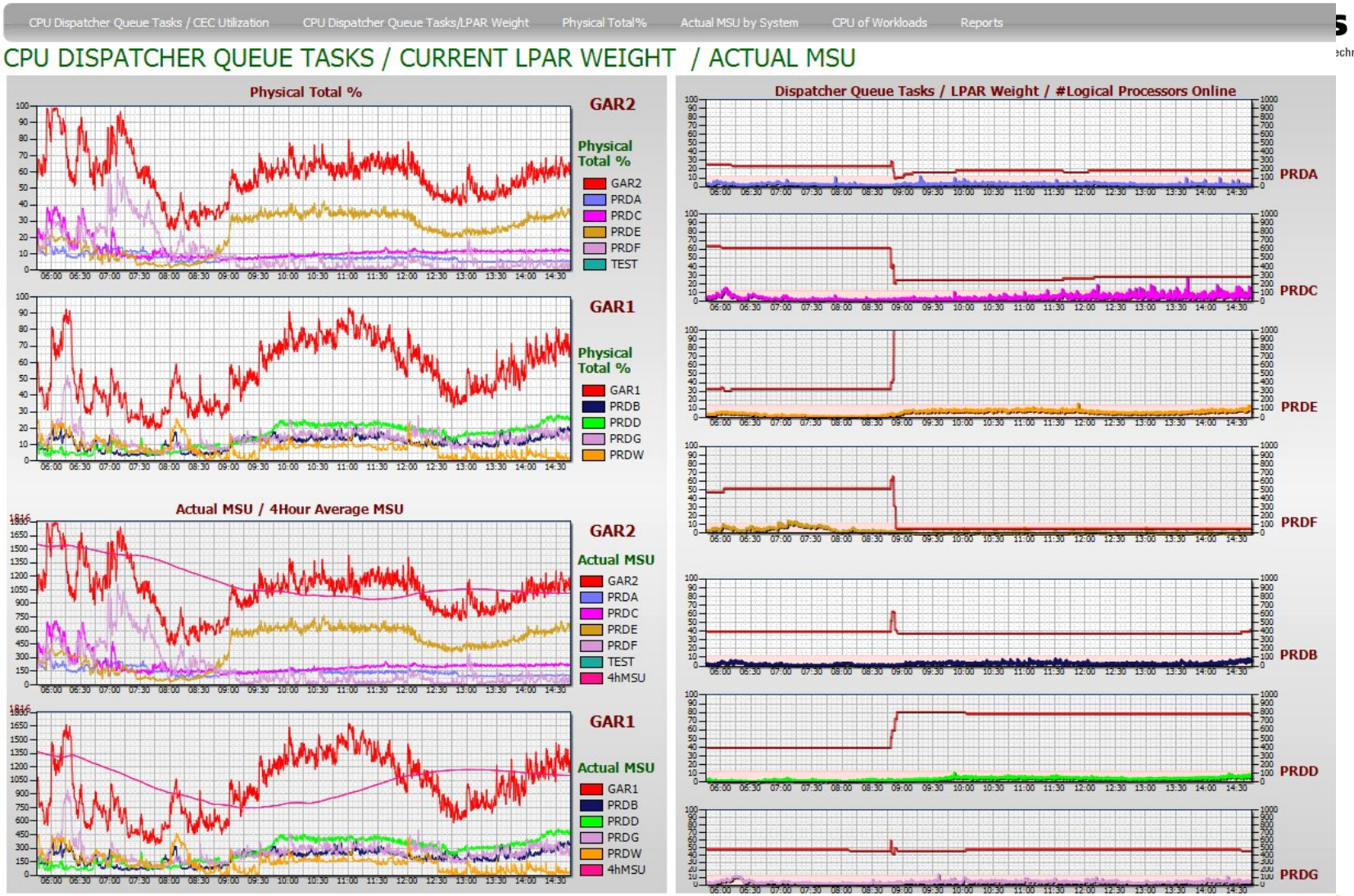
Z196 Online Time ALL Trx Avg ResponseTime 0.0036



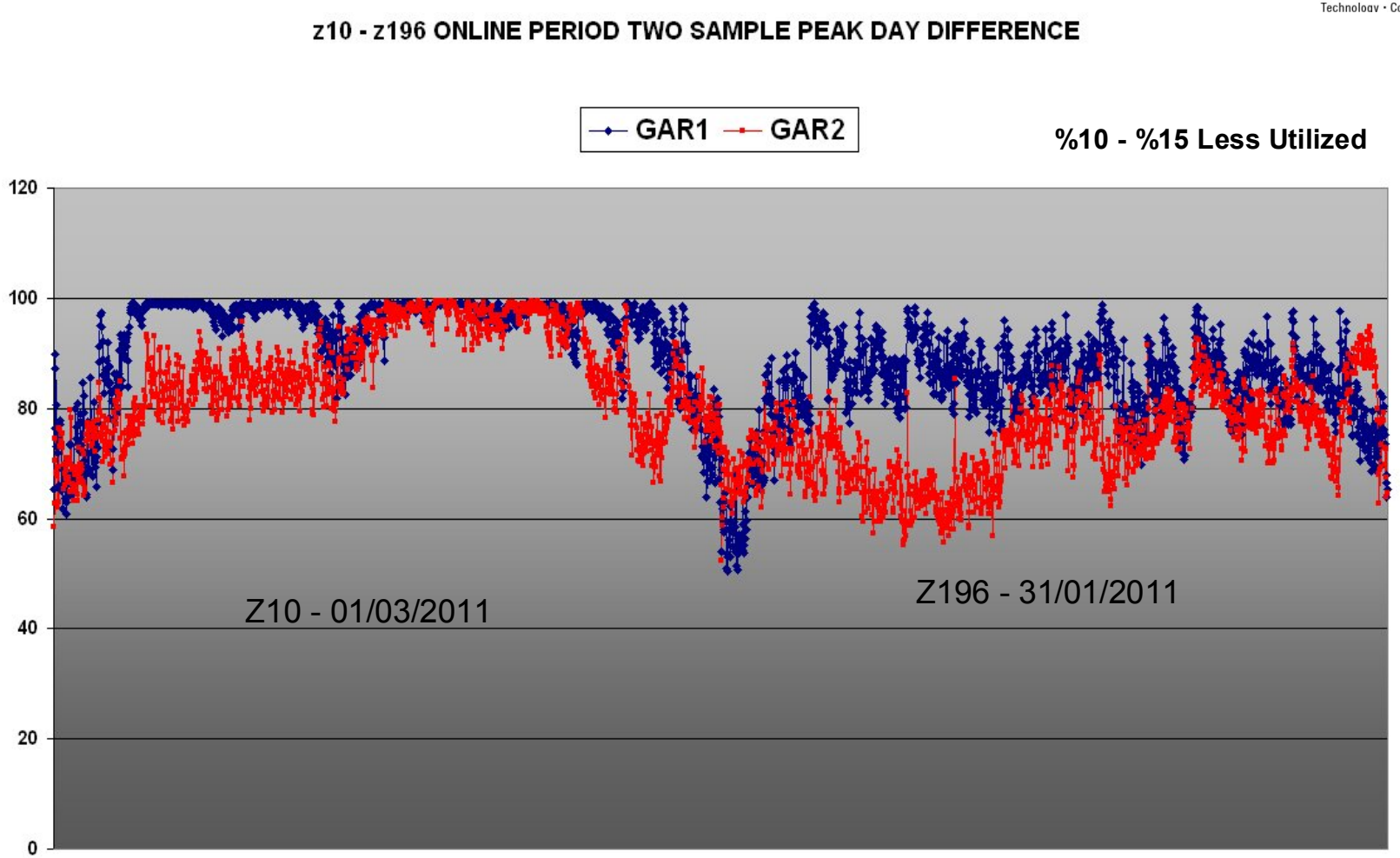
Z10 To z196 – Online Workload View



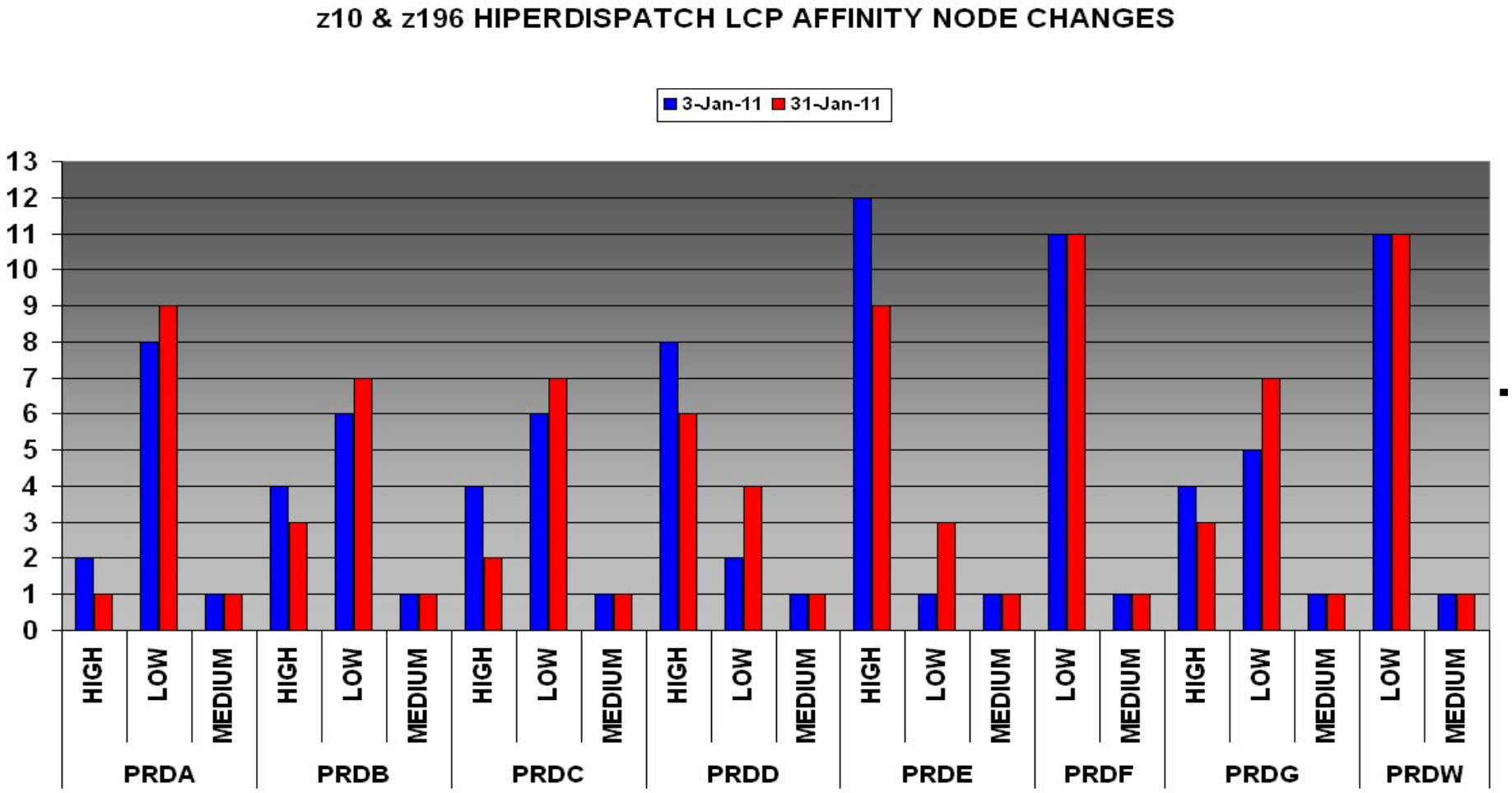
CEC UTILIZATION PANEL



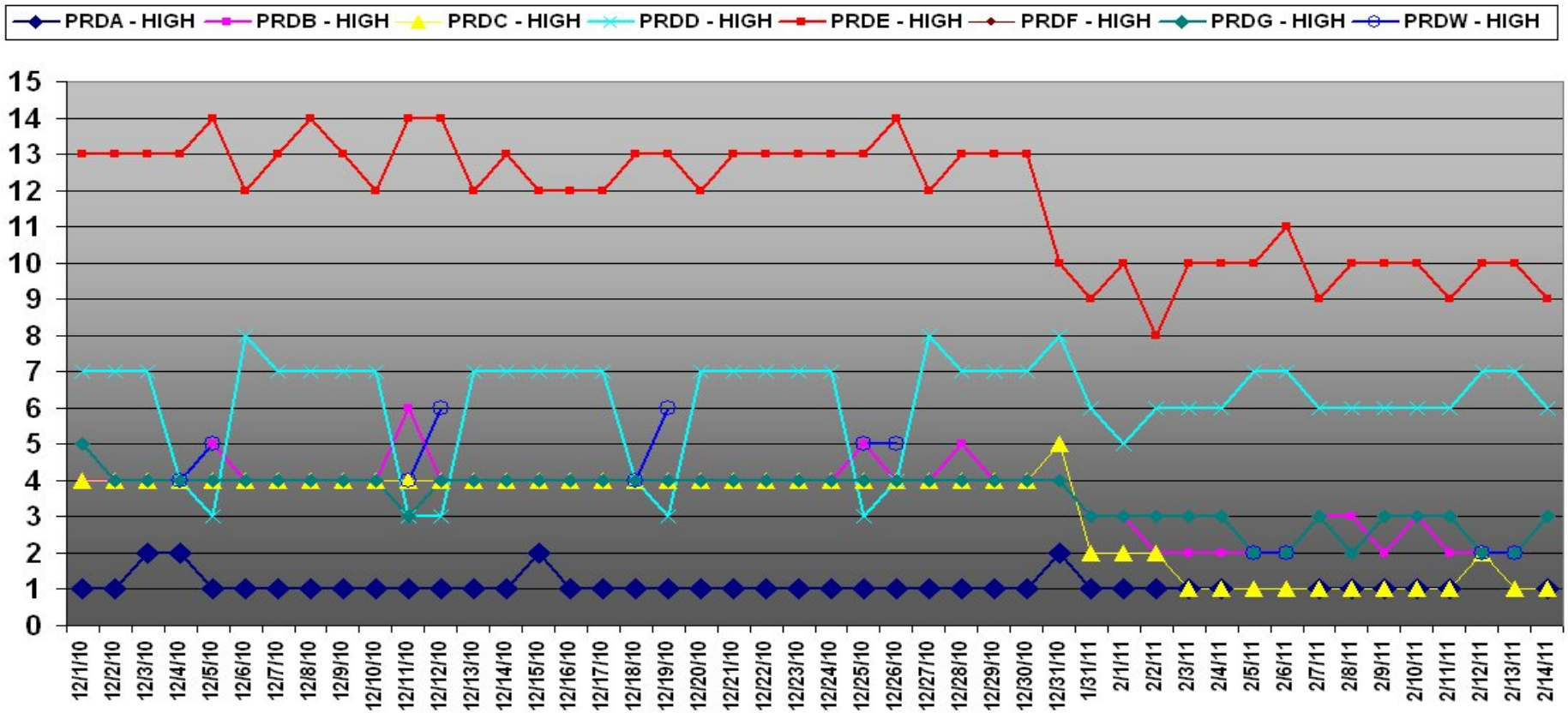
Z10 To z196 – CEC Utilization



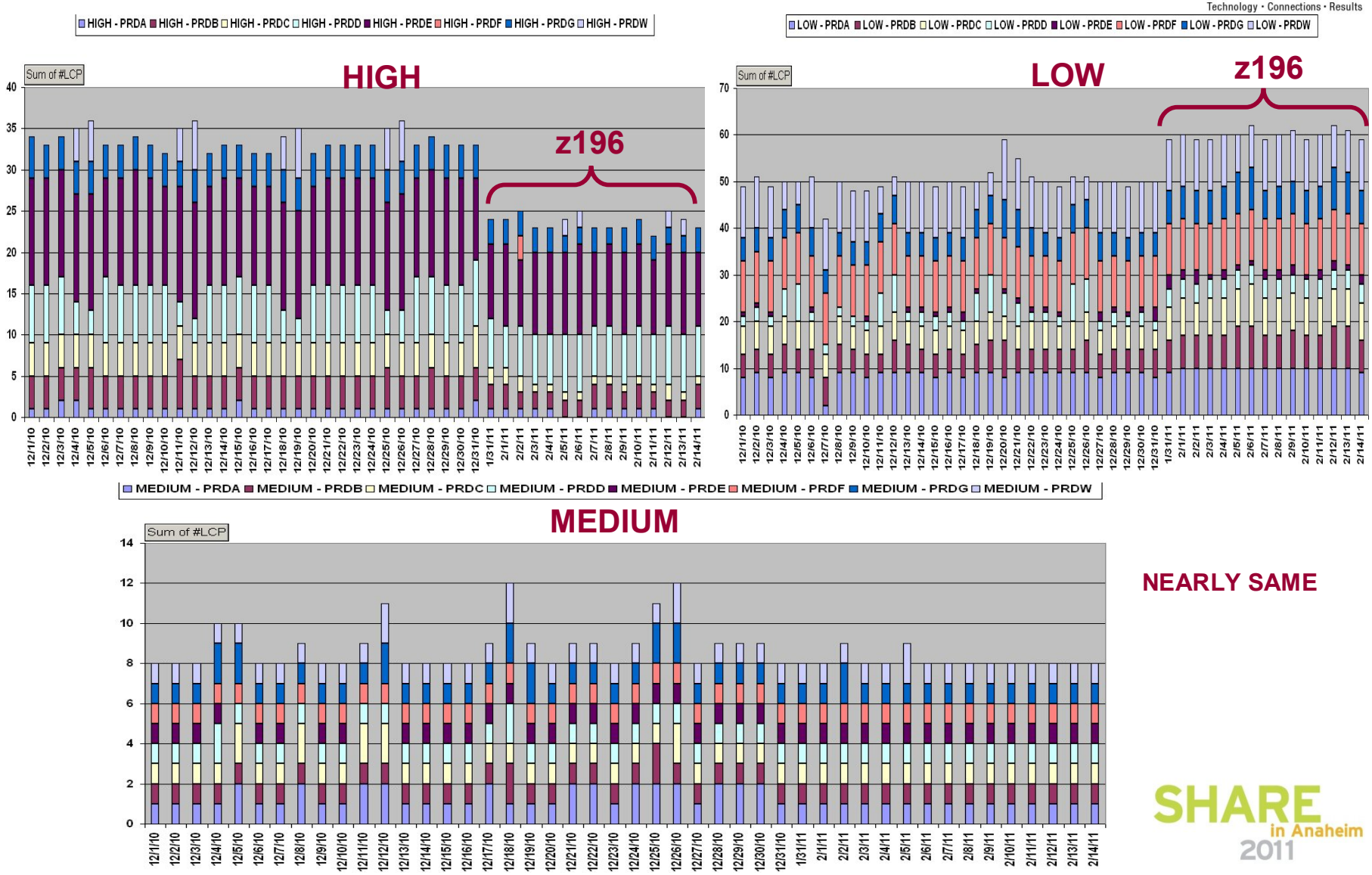
Z10 To z196 – HD Affinity Changes



Z10 To z196 – HD Affinity Changes

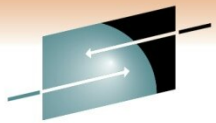


Z10 To z196 – HD Affinity Changes



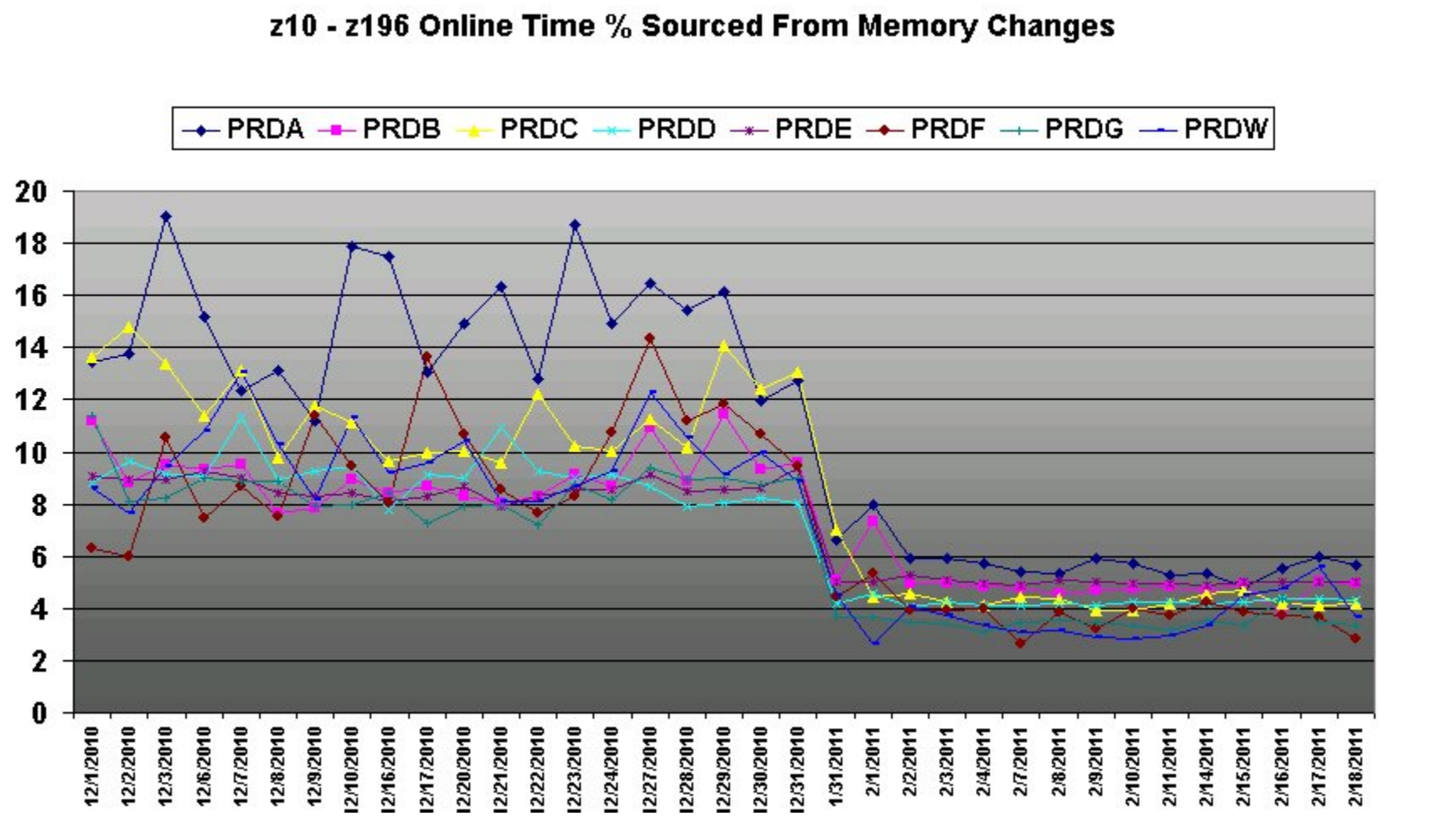
NEARLY SAME

Z10 To z196 – % Sourced From Memory Changes

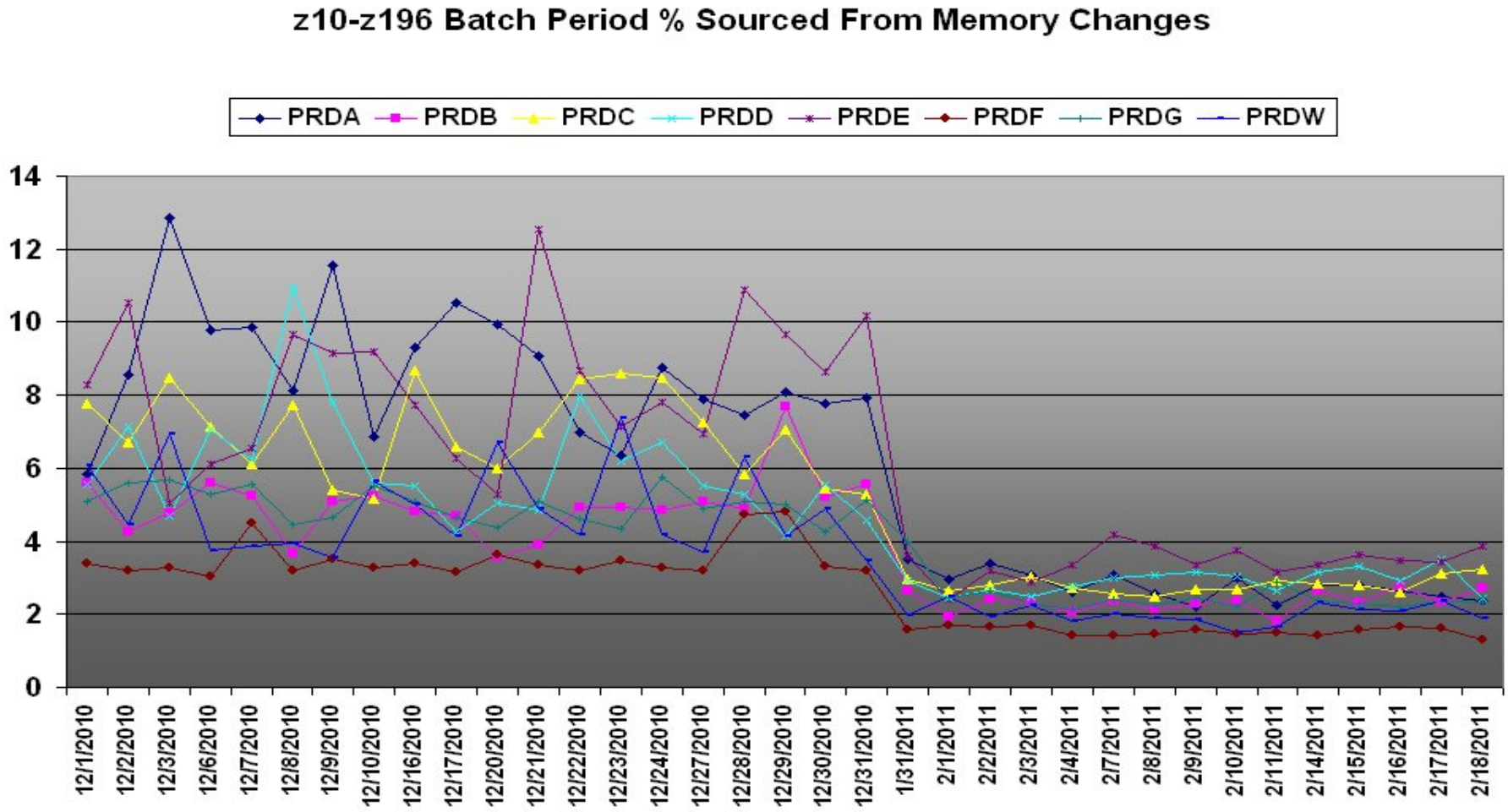


BATCH				ONLINE			
SYSTEM	z10MEMP	z196MEMP	%Decrease	SYSTEM	z10MEMP	z196MEMP	%Decrease
PRDA	8.69	2.78	67.98	PRDA	14.90	5.82	60.93
PRDB	4.98	2.34	53.06	PRDB	9.14	4.95	45.89
PRDC	6.97	2.80	59.77	PRDC	11.63	4.47	61.52
PRDD	6.04	2.90	51.95	PRDD	9.05	4.24	53.12
PRDE	8.35	3.43	58.98	PRDE	8.65	5.02	42.01
PRDF	3.50	1.54	56.17	PRDF	9.62	3.83	60.15
PRDG	5.01	2.49	50.25	PRDG	8.56	3.49	59.17
PRDW	4.88	2.01	58.75	PRDW	9.72	3.68	62.10
Average	6.05	2.54	58.09	Average	10.16	4.44	56.30

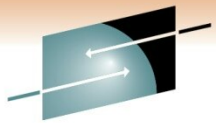
Z10 To z196 – % Sourced From Memory Changes



Z10 To z196 – % Sourced From Memory Changes



Z10 To z196 Estimated Complexity Cycle Per Instruction

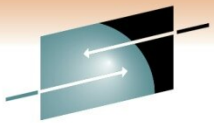


- **Expected To Be Decreased With z196 Upgrade Because Of Out Of Order Execution Feature**

BATCH				ONLINE			
SYSTEM	z10ESTICCPI	z196ESTICCPI	%Decrease	SYSTEM	z10ESTICCPI	z196ESTICCPI	%Decrease
PRDA	2.09	3.09	-47.87	PRDA	1.20	2.72	-127.58
PRDB	3.13	2.95	5.69	PRDB	2.76	2.51	9.16
PRDC	2.90	3.23	-11.37	PRDC	3.02	3.43	-13.60
PRDD	3.11	2.98	4.05	PRDD	3.49	3.53	-1.11
PRDE	2.03	3.11	-53.26	PRDE	3.23	3.05	5.68
PRDF	3.39	3.24	4.35	PRDF	2.61	2.79	-6.72
PRDG	3.21	2.69	16.16	PRDG	3.12	2.67	14.31
PRDW	2.72	2.87	-5.78	PRDW	2.88	2.60	9.73
Average	2.82	3.02	-7.07	Average	2.79	2.91	-4.43

This calculation does not show DECREASE!.
THE REASON is : There are NEGATIVE values in ESTICCPI because of Low Utilization Effect

Z10 To z196 Estimated Complexity Cycle Per Instruction



- **When Negative ESTICCPI values removed from calculations, The real change in ESTICCPI value by moving from z10s To z196s is 10% Decrease. THIS SHOWS THE EFFECT OF OUT OF ORDER EXECUTION Feature.**

BATCH				ONLINE			
SYSTEM	z10ESTICCPI	z196ESTICCPI	Decrease%	SYSTEM	z10ESTICCPI	z196ESTICCPI	Decrease%
PRDA	3.45	3.15	8.52	PRDA	3.58	3.21	10.46
PRDB	3.31	2.96	10.38	PRDB	3.03	2.77	8.65
PRDC	3.64	3.24	11.05	PRDC	3.73	3.44	7.71
PRDD	3.35	2.99	10.70	PRDD	3.63	3.54	2.53
PRDE	3.30	3.06	7.17	PRDE	3.23	3.05	5.71
PRDF	3.57	3.27	8.45	PRDF	3.47	2.79	19.59
PRDG	3.21	2.84	11.74	PRDG	3.18	2.66	16.30
PRDW	3.05	2.82	7.66	PRDW	3.01	2.64	12.37
Average	3.36	3.04	9.46	Average	3.36	3.01	10.42

- **IBMs Expection is 10-15% Decrease.But This Value is ESTIMATION.**

Z10 To z196 Estimated Cycle Per L1 Miss

BATCH				ONLINE			
SYSTEM	z10ESTSCP1M	z196ESTSCP1M	%Decrease	SYSTEM	z10ESTSCP1M	z196ESTSCP1M	%Decrease
PRDA	95.92	50.54	47.31	PRDA	157.75	77.52	50.86
PRDB	67.95	42.28	37.78	PRDB	111.85	64.00	42.79
PRDC	87.49	50.83	41.90	PRDC	136.08	74.79	45.04
PRDD	76.51	46.91	38.68	PRDD	115.03	63.13	45.12
PRDE	91.52	49.99	45.38	PRDE	121.66	64.75	46.77
PRDF	64.16	38.16	40.53	PRDF	130.16	61.70	52.60
PRDG	75.96	47.30	37.73	PRDG	115.68	61.72	46.65
PRDW	73.68	42.86	41.83	PRDW	139.47	64.64	53.65
Average	79.15	46.11	41.74	Average	128.46	66.53	48.21

Z10 To z196 TLB1 Miss

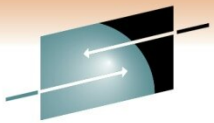
- With z196 , There Are 2 TLBs, TLB1 & TLB2. This shows TLB1Miss
- Batch & Online Workload TLB1Miss Values Are Very Different

BATCH				ONLINE			
SYSTEM	z10TLB1MISS	z196TLB1MISS	%Decrease	SYSTEM	z10TLB1MISS	z196TLB1MISS	%Decrease
PRDA	21.22	9.17	56.78	PRDA	32.02	14.40	55.04
PRDB	18.73	7.80	58.36	PRDB	28.56	12.86	54.98
PRDC	21.98	10.35	52.90	PRDC	33.49	15.15	54.76
PRDD	20.09	9.42	53.11	PRDD	31.44	14.36	54.33
PRDE	19.20	7.88	58.96	PRDE	30.20	12.92	57.23
PRDF	15.93	6.17	61.24	PRDF	25.86	11.02	57.40
PRDG	21.99	9.74	55.68	PRDG	29.47	12.92	56.16
PRDW	17.04	7.21	57.67	PRDW	25.98	11.07	57.38
Average	19.52	8.47	56.62	Average	29.63	13.09	55.83

2 TLB usage started with z9s

Z10 To z196 Upgrade IBM Analiz

Z10 To z196 Upgrade IBM Analiz



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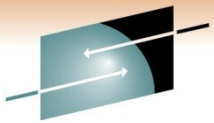
z196 Serial 60E26 – PRDA, PRDC, PRDE, PRDF

Machine	SYSID	Mon	Day	SH	Hour	CPI	Prb State	Est Instr Cmplx CPI	Est Finite CPI	Est SCPL1M	L1MP	L15P / L2P	L3P	L2LP / L4LP	L2RP / L4RP	MEMP	Rel Nest Intensity	LPARCPU	Eff GHz	LSPR Wkld Hint
z10 722	PRDA	NOV	22	P	TOTAL	11.52	35.1	3.77	7.75	129	6.0	67.3	0.0	19.4	3.0	10.4	1.04	269.3	4.4	HIGH
z10 724	PRDA	JAN	3	P	TOTAL	10.04	44.1	3.51	6.53	126	5.2	67.8	0.0	19.1	2.8	10.3	1.03	247.6	4.4	HIGH
z10 724	PRDA	JAN	17	P	TOTAL	9.99	43.4	3.54	6.46	131	4.9	68.4	0.0	17.7	3.2	10.8	1.06	296.4	4.4	HIGH
						10.52	**40.8**	**3.61**	**6.91**	**129**	**5.4**	**67.8**	**0.0**	**18.7**	**3.0**	**10.5**	**1.04**	**271.1**		
z196 717	PRDA	JAN	31	P	TOTAL	6.83	43.5	2.73	4.10	81	5.1	56.9	22.7	10.4	5.6	4.5	1.06	105.6	5.2	HIGH
z196 717	PRDA	FEB	1	P	TOTAL	6.86	48.3	2.84	4.03	81	5.0	57.7	23.0	12.3	1.2	5.8	1.08	98.2	5.2	HIGH
						6.85	**45.9**	**2.79**	**4.07**	**81**	**5.0**	**57.3**	**22.9**	**11.3**	**3.4**	**5.1**	**1.07**	**101.9**		
		Relative Capacity Ratio				**1.82**														
z10 722	PRDC	NOV	22	P	TOTAL	12.98	30.5	3.80	9.18	149	6.1	60.7	0.0	24.5	2.6	12.2	1.22	372.2	4.4	HIGH
z10 724	PRDC	JAN	3	P	TOTAL	12.24	33.3	3.75	8.49	143	6.0	62.8	0.0	23.2	2.1	11.9	1.17	342.2	4.4	HIGH
z10 724	PRDC	JAN	17	P	TOTAL	11.59	31.3	3.65	7.94	140	5.7	63.4	0.0	23.0	2.3	11.4	1.14	428.6	4.4	HIGH
						12.27	**31.7**	**3.73**	**8.54**	**144**	**5.9**	**62.3**	**0.0**	**23.6**	**2.3**	**11.8**	**1.18**	**381.0**		
z196 717	PRDC	JAN	31	P	TOTAL	8.31	34.1	3.25	5.06	82	6.2	54.5	27.4	10.2	2.3	5.6	1.10	224.9	5.2	HIGH
z196 717	PRDC	FEB	1	P	TOTAL	6.40	29.8	3.01	3.38	70	4.8	58.3	24.5	8.2	5.4	3.6	0.92	247.3	5.2	AVG
						7.36	**31.9**	**3.13**	**4.22**	**76**	**5.5**	**56.4**	**26.0**	**9.2**	**3.9**	**4.6**	**1.01**	**236.1**		
		Relative Capacity Ratio				**1.97**														
z10 722	PRDE	NOV	22	P	TOTAL	10.70	51.8	3.30	7.40	153	4.8	62.3	0.0	24.7	2.1	11.0	1.12	1015.1	4.4	HIGH
z10 724	PRDE	JAN	3	P	TOTAL	8.84	49.3	3.20	5.64	120	4.7	66.7	0.0	22.4	2.0	8.9	0.94	884.4	4.4	AVG
z10 724	PRDE	JAN	17	P	TOTAL	9.86	50.7	3.27	6.59	134	4.9	62.9	0.0	24.3	2.9	9.9	1.06	974.2	4.4	HIGH
						9.80	**50.6**	**3.26**	**6.54**	**136**	**4.8**	**63.9**	**0.0**	**23.8**	**2.3**	**9.9**	**1.04**	**957.9**		
z196 717	PRDE	JAN	31	P	TOTAL	6.17	51.5	2.86	3.31	69	4.8	60.7	25.5	8.1	0.7	5.0	0.92	526.7	5.2	AVG
z196 717	PRDE	FEB	1	P	TOTAL	6.11	50.5	2.92	3.18	67	4.8	61.5	25.0	7.8	0.7	5.0	0.91	472.7	5.2	AVG
						6.14	**51.0**	**2.89**	**3.25**	**68**	**4.8**	**61.1**	**25.2**	**7.9**	**0.7**	**5.0**	**0.92**	**499.7**		
		Relative Capacity Ratio				**1.89**														
z10 722	PRDF	NOV	22	P	TOTAL	6.48	46.0	3.08	3.40	138	2.5	69.9	0.0	16.2	4.0	9.9	1.00	122.0	4.4	AVG
z10 724	PRDF	JAN	3	P	TOTAL	7.19	18.9	3.54	3.64	143	2.5	67.3	0.0	17.4	4.3	11.0	1.10	246.9	4.4	AVG
z10 724	PRDF	JAN	17	P	TOTAL	7.12	29.8	3.65	3.47	99	3.5	75.9	0.0	14.1	3.9	6.2	0.70	326.4	4.4	AVG
						6.93	**31.6**	**3.42**	**3.50**	**127**	**2.8**	**71.0**	**0.0**	**15.9**	**4.1**	**9.0**	**0.93**	**231.8**		
z196 717	PRDF	JAN	31	P	TOTAL	5.11	27.7	3.04	2.07	58	3.6	68.5	16.2	10.8	1.4	3.1	0.71	72.3	5.2	AVG
z196 717	PRDF	FEB	1	P	TOTAL	4.88	20.2	3.02	1.86	52	3.6	71.9	13.9	10.2	1.3	2.7	0.63	173.1	5.2	AVG
						5.00	**24.0**	**3.03**	**1.97**	**55**	**3.6**	**70.2**	**15.1**	**10.5**	**1.4**	**2.9**	**0.67**	**122.7**		
		Relative Capacity Ratio				**1.64**														

Z10 To z196 Upgrade IBM Analiz



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z196 Serial 60E16 – PRDB, PRDD, PRDG, PRDW

Machine	SYSID	Mon	Day	SH	Hour	CPI	Prb State	Est Instr Cmplx CPI	Est Finite CPI	Est SCPL1M	L1MP	L15P / L2P	L3P	L2LP / L4LP	L2RP / L4RP	MEMP	Rel Nest Intensity	LPARCPU	Eff GHz	LSPR Wkld Hint
z10 722	PRDB	NOV	22	P	TOTAL	8.10	40.4	3.09	5.00	120	4.2	69.6	0.0	19.4	1.2	9.9	0.96	419.7	4.4	AVG
z10 722	PRDB	JAN	3	P	TOTAL	7.47	35.6	3.18	4.29	108	4.0	71.5	0.0	18.4	1.3	8.9	0.88	432.5	4.4	AVG
z10 722	PRDB	JAN	17	P	TOTAL	6.82	30.0	2.89	3.94	112	3.5	70.1	0.0	19.3	1.4	9.3	0.92	505.4	4.4	AVG
						7.46	**35.3**	**3.05**	**4.41**	**113**	**3.9**	**70.4**	**0.0**	**19.0**	**1.3**	**9.3**	**0.92**	**452.5**		
z196 717	PRDB	JAN	31	P	TOTAL	5.61	40.7	2.57	3.04	69	4.4	62.7	22.4	8.7	1.2	4.9	0.92	274.5	5.2	AVG
z196 717	PRDB	FEB	1	P	TOTAL	5.50	39.0	2.58	2.92	68	4.3	63.0	22.7	8.3	1.1	4.9	0.91	266.8	5.2	AVG
						5.56	**39.9**	**2.58**	**2.98**	**69**	**4.4**	**62.9**	**22.6**	**8.5**	**1.2**	**4.9**	**0.92**	**270.7**		
		Relative Capacity Ratio				**1.59**														
z10 722	PRDD	NOV	22	P	TOTAL	10.98	35.9	3.73	7.25	119	6.1	63.9	0.0	24.8	2.6	8.6	0.96	770.0	4.4	HIGH
z10 722	PRDD	JAN	3	P	TOTAL	9.97	38.7	3.67	6.30	107	5.9	66.9	0.0	23.3	1.9	7.9	0.87	679.5	4.4	AVG
z10 722	PRDD	JAN	17	P	TOTAL	9.65	41.9	3.62	6.03	109	5.5	66.4	0.0	23.6	1.9	8.1	0.89	691.2	4.4	AVG
						10.20	**38.8**	**3.67**	**6.53**	**112**	**5.8**	**65.8**	**0.0**	**23.9**	**2.1**	**8.2**	**0.91**	**713.6**		
z196 717	PRDD	JAN	31	P	TOTAL	7.90	40.2	3.40	4.51	68	6.6	57.8	25.9	11.6	0.6	4.2	0.88	516.9	5.2	HIGH
z196 717	PRDD	FEB	1	P	TOTAL	7.79	40.3	3.37	4.42	68	6.5	58.8	25.0	11.3	0.7	4.3	0.88	440.1	5.2	HIGH
						7.85	**40.3**	**3.39**	**4.47**	**68**	**6.6**	**58.3**	**25.4**	**11.4**	**0.6**	**4.2**	**0.88**	**478.5**		
		Relative Capacity Ratio				**1.54**														
z10 722	PRDG	NOV	22	P	TOTAL	9.10	30.9	3.28	5.82	137	4.2	67.1	0.0	20.9	2.0	10.0	1.01	512.6	4.4	HIGH
z10 722	PRDG	JAN	3	P	TOTAL	6.81	27.3	2.87	3.94	112	3.5	70.2	0.0	19.3	1.6	9.0	0.90	507.1	4.4	AVG
z10 722	PRDG	JAN	17	P	TOTAL	7.67	32.3	2.99	4.68	116	4.0	69.1	0.0	19.7	1.9	9.3	0.94	505.4	4.4	AVG
						7.86	**30.2**	**3.05**	**4.81**	**122**	**3.9**	**68.8**	**0.0**	**20.0**	**1.8**	**9.4**	**0.95**	**508.4**		
z196 717	PRDG	JAN	31	P	TOTAL	5.45	34.8	2.58	2.87	65	4.4	63.0	22.6	6.4	4.4	3.6	0.85	306.3	5.2	AVG
z196 717	PRDG	FEB	1	P	TOTAL	5.11	32.7	2.47	2.63	65	4.1	62.9	22.6	6.4	4.4	3.6	0.85	291.9	5.2	AVG
						5.28	**33.7**	**2.53**	**2.75**	**65**	**4.2**	**63.0**	**22.6**	**6.4**	**4.4**	**3.6**	**0.85**	**299.1**		
		Relative Capacity Ratio				**1.76**														
z10 722	PRDW	NOV	22	P	TOTAL	6.18	29.4	2.69	3.49	141	2.5	66.1	0.0	20.1	4.4	9.4	1.01	152.6	4.4	AVG
z10 722	PRDW	JAN	3	P	TOTAL	7.10	36.1	3.19	3.91	124	3.2	68.8	0.0	18.8	3.7	8.7	0.93	130.5	4.4	AVG
z10 722	PRDW	JAN	17	P	TOTAL	5.66	36.7	2.97	2.69	92	2.9	75.4	0.0	15.4	4.0	5.3	0.64	252.9	4.4	LOW
						6.31	**34.0**	**2.95**	**3.36**	**119**	**2.8**	**70.1**	**0.0**	**18.1**	**4.0**	**7.8**	**0.86**	**178.7**		
z196 717	PRDW	JAN	31	P	TOTAL	5.06	31.2	2.77	2.30	67	3.4	62.4	20.1	11.2	2.8	3.5	0.83	84.7	5.2	AVG
z196 717	PRDW	FEB	1	P	TOTAL	4.33	47.8	2.51	1.82	57	3.2	65.9	17.9	11.1	2.8	2.3	0.67	250.8	5.2	AVG
						4.70	**39.5**	**2.64**	**2.06**	**62**	**3.3**	**64.2**	**19.0**	**11.1**	**2.8**	**2.9**	**0.75**	**167.8**		
		Relative Capacity Ratio				**1.59**														

Z10 To z196 Upgrade IBM Analiz

- **LSPR Multi Image Table**
  - Average Workload z10 722 Vs z196 717 – **1.44 Expectation**
  - Average Workload z10 724 Vs z196 717 – **1.47 Expectation**

- **z196 60E26**
  - Overall All LPARs CPU/DASD EXCP **1.78** Vs z10
  - Averaged 20% less busy than z10
    - Backing out Low Utilization Effect 10% = **1.62** Vs z10
  - ~12% better than z10 722 expectation 1.44
  - ~10% better than z10 724 expectation 1.47

- **z196 60E16**
  - Overall All LPARs CPU/DASD EXCP **1.71** Vs z10
  - Averaged 10% less busy than z10
    - Backing out Low Utilization Effect 5% = **1.63** Vs z10
  - ~ 13% better than expectation 1.44

- **Overall Estimate that the 2 z196s delivered ~10% better than Expectation**

References

- IBM ResourceLink Documents SA23-2261-01 & SA23-2260-01
- IBM Research Documents
  - IBM System z10 processor cache subsystem microarchitecture
  - Design and microarchitecture of the IBM System z10 microprocessor
- IBM zEnterprise z196 Technical Guide Redbook
- IBM Z/OS 1.12 Implementation Redbook
- IBM ResourceLink LSPR Website
- http://www.redbooks.ibm.com/redpieces/pdfs/redp4727.pdf

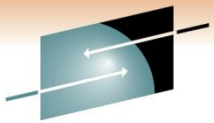
Looking Forward To IBM Research"s z196 Papers

Special Thanks To

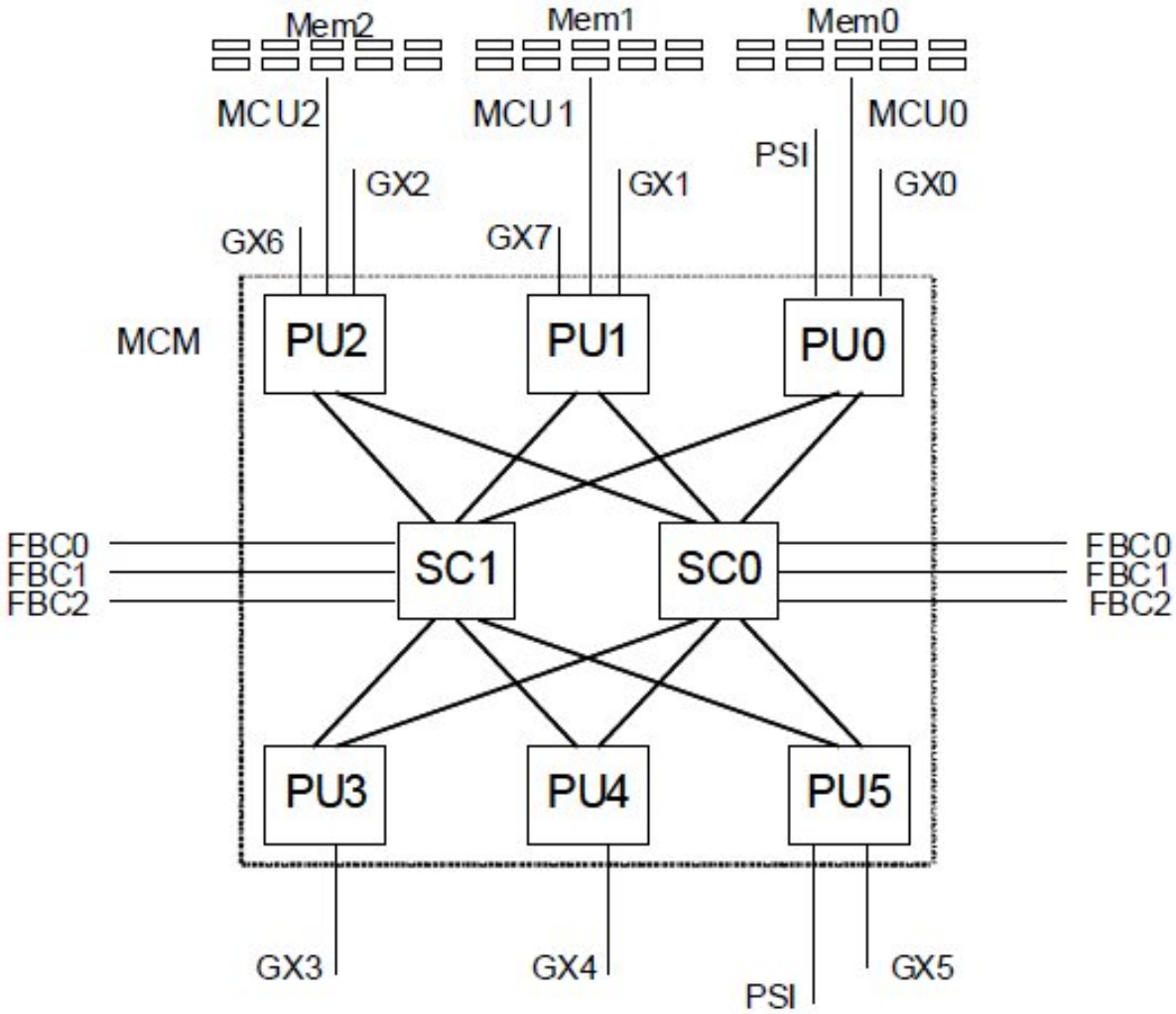
Gary King

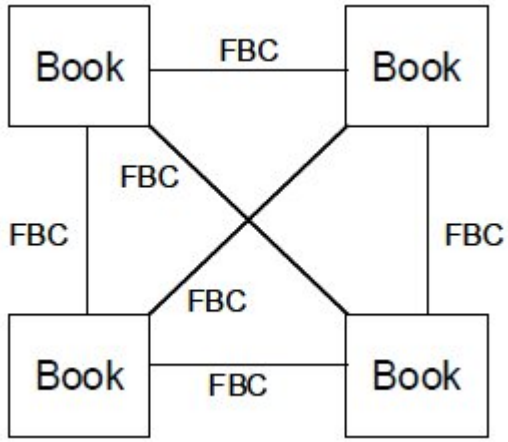
John Burg

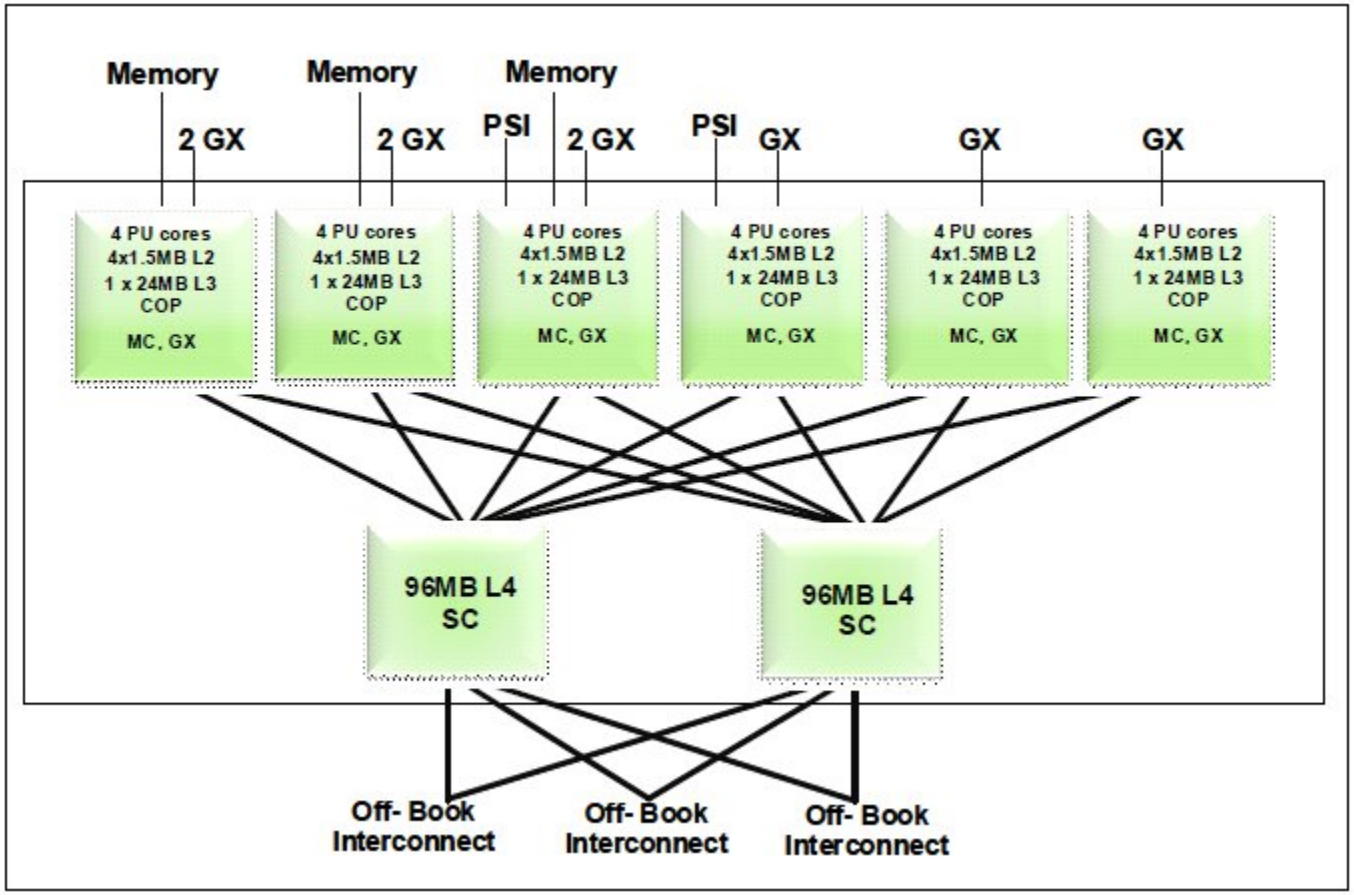
Backup

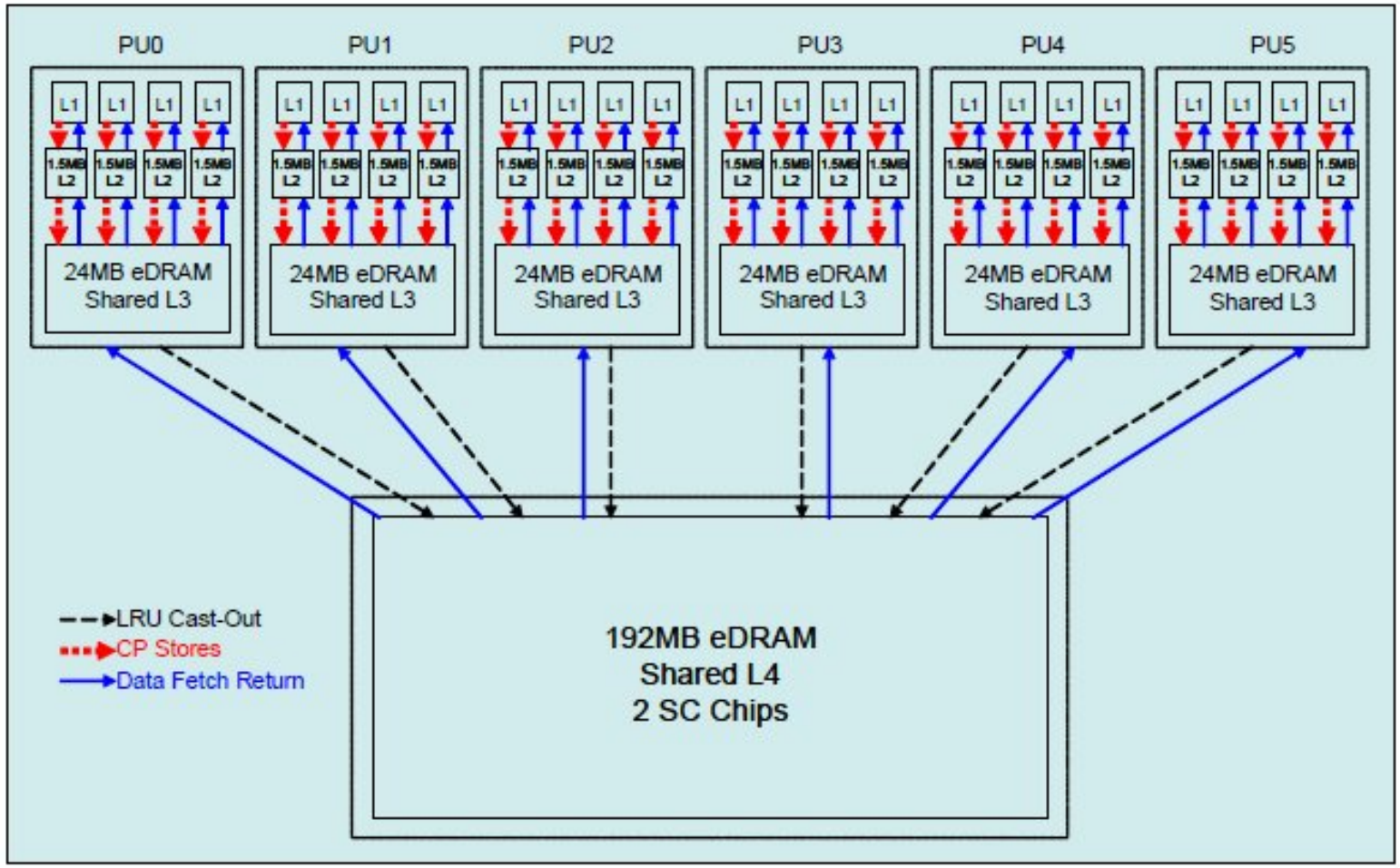


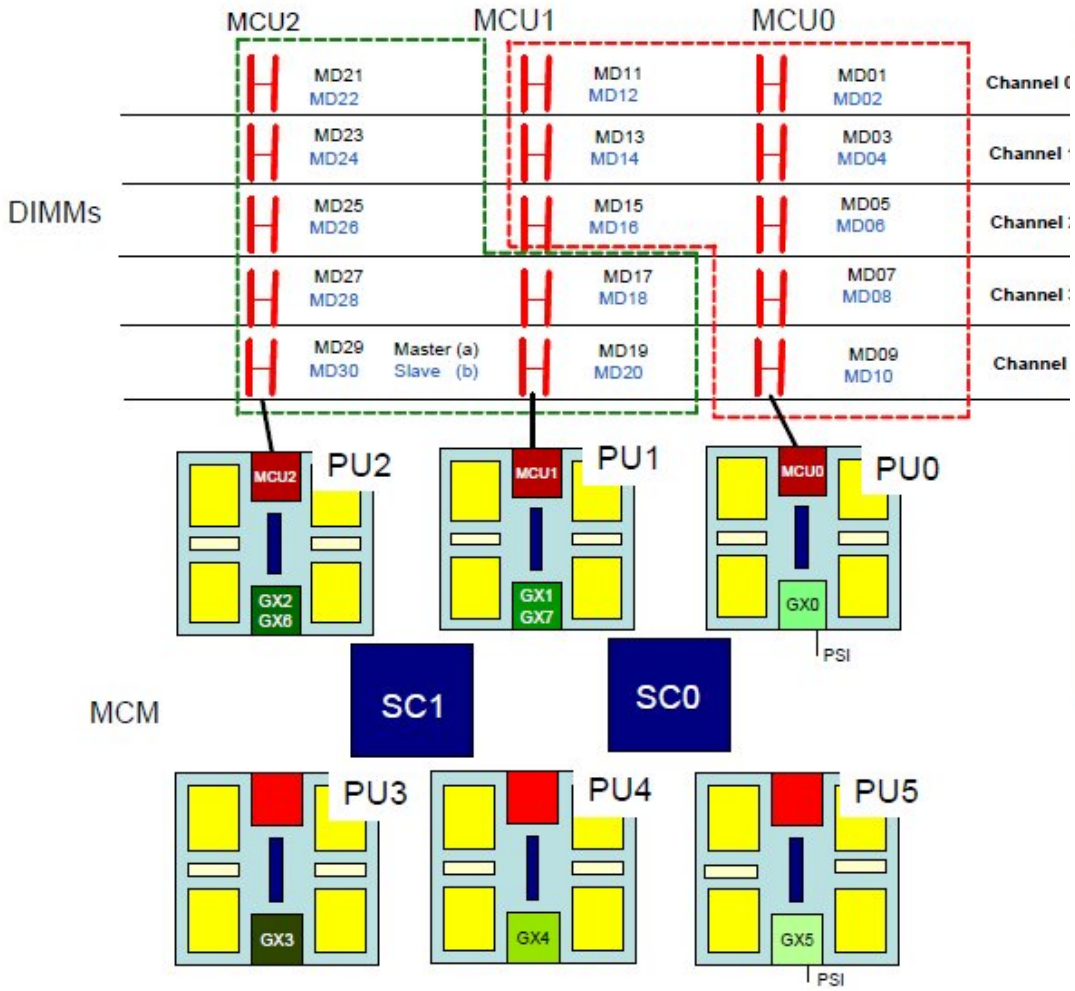
Cache Design

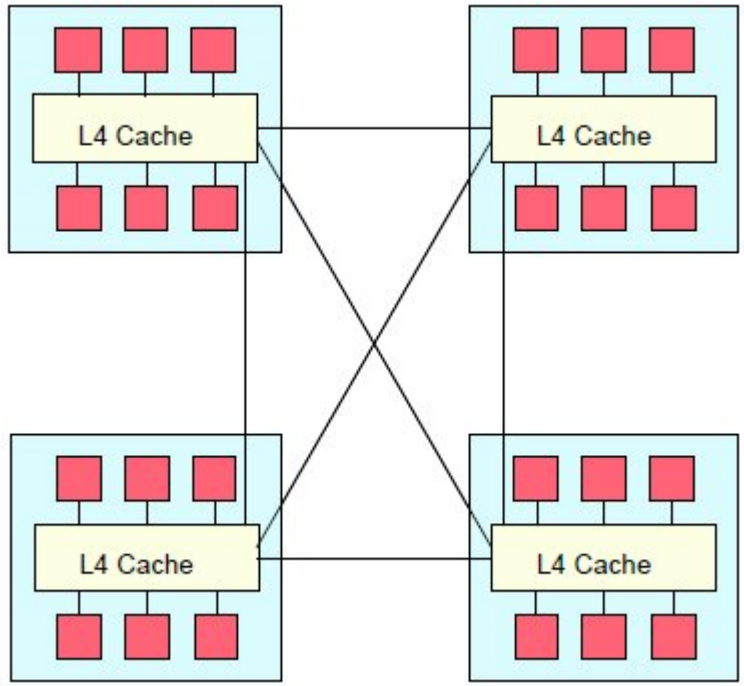


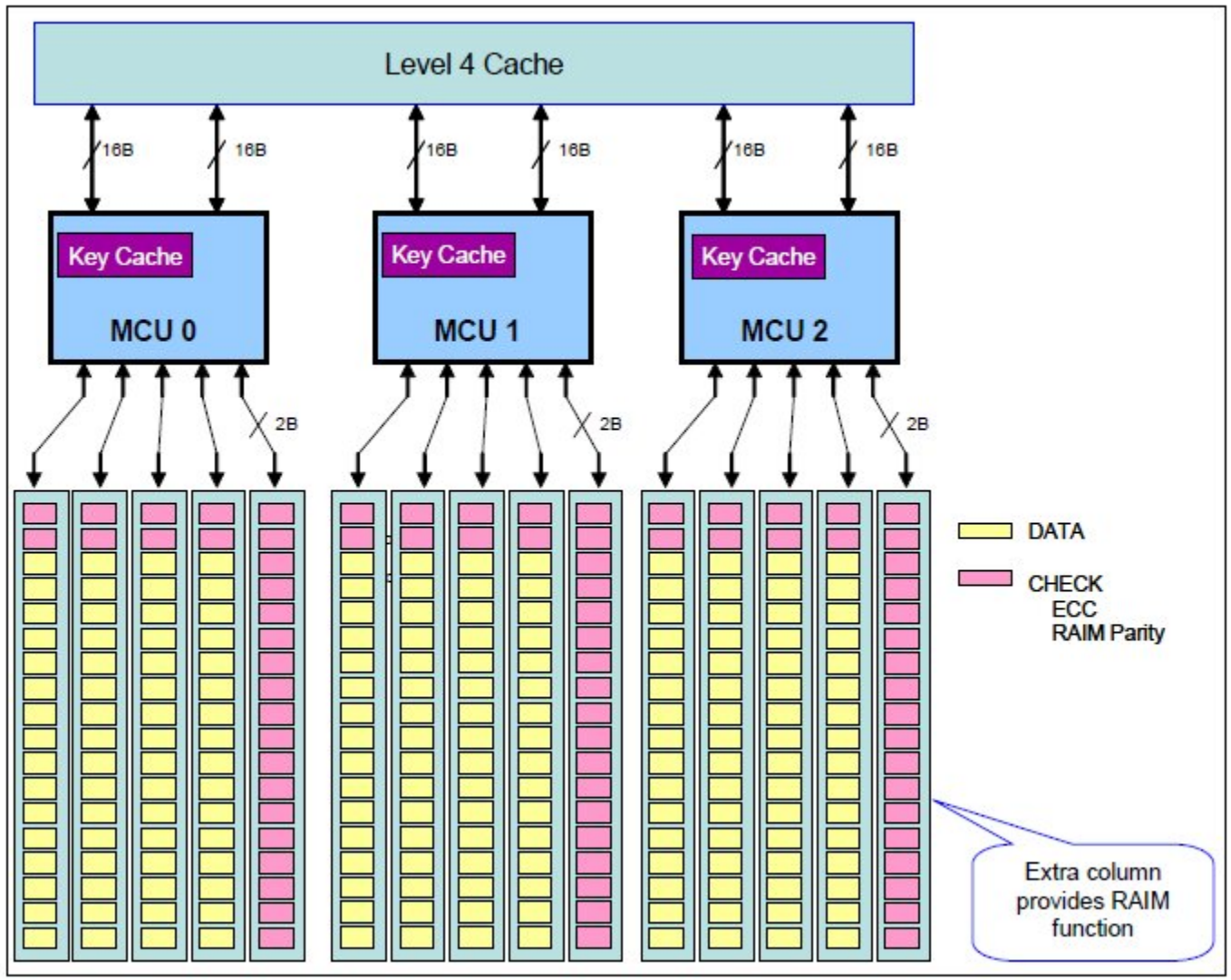


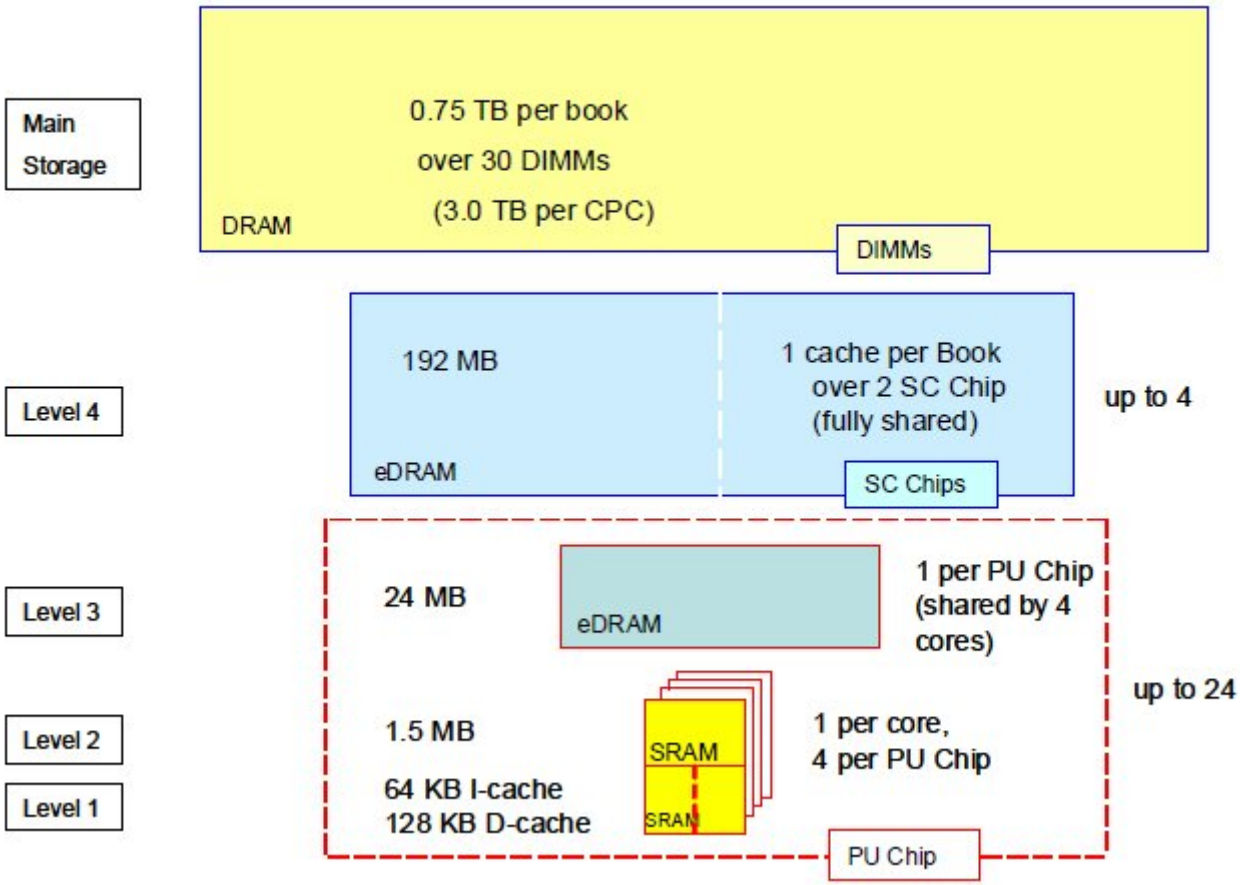

Memory
Memory
Memory
2 GX
2 GX
PSI
2 GX
PSI
GX
GX
GX
4 PU cores
4x1.5MB L2
1 x 24MB L3
COP
MC, GX
96MB L4
SC
96MB L4
SC
Off- Book
Interconnect
Off- Book
Interconnect
Off- Book
Interconnect


PU0
PU1
PU2
PU3
PU4
PU5
L1
1.5MB L2
24MB eDRAM Shared L3
192MB eDRAM
Shared L4
2 SC Chips
LRU Cast-Out
CP Stores
Data Fetch Return


MCU2
MCU1
MCU0
DIMMs
MD21
MD22
MD11
MD12
MD01
MD02
Channel
MD23
MD24
MD13
MD14
MD03
MD04
MD25
MD26
MD15
MD16
MD05
MD06
MD27
MD28
MD17
MD18
MD07
MD08
MD29
MD30
Master (a)
Slave (b)
MD19
MD20
MD09
MD10
PU2
PU1
PU0
MCU2
MCU1
MCU0
GX2
GX6
GX1
GX7
GX0
PSI
MCM
SC1
SC0
PU3
PU4
PU5
GX3
GX4
GX5
PSI


L4 Cache
L4 Cache
L4 Cache
L4 Cache


Level 4 Cache
16B
16B
16B
16B
16B
16B
Key Cache
MCU 0
Key Cache
MCU 1
Key Cache
MCU 2
2B
2B
2B
DATA
CHECK
ECC
RAIM Parity
Extra column provides RAIM function


Main Storage
0.75 TB per book
over 30 DIMMs
(3.0 TB per CPC)
DRAM
DIMMs
Level 4
192 MB
eDRAM
1 cache per Book
over 2 SC Chip
(fully shared)
SC Chips
up to 4
Level 3
24 MB
eDRAM
1 per PU Chip
(shared by 4
cores)
Level 2
1.5 MB
SRAM
1 per core,
4 per PU Chip
Level 1
64 KB I-cache
128 KB D-cache
SRAM
PU Chip
up to 24